Rapid Characterization Method for New Semiconductor Processes

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Abstract—Having adequate characterization of new semiconductor processes is important in the development of integrated circuits (ICs) destined for mil/aero systems. In the past, designers have had to rely upon the fidelity of models found in the Process Design Kit (PDK). For new processes, these models can be incomplete or not fully characterized by the foundry. With Mil/Aero applications, the performance data can be inadequate when designing components for harsh environments. Harsh environments can include extreme temperatures and damaging effects of radiation exposure.

A new methodology for evaluating key parameters to determine the process's suitability for a particular application is described. The new methodology described incorporates a unique combination of hardware and software to provide extended characterization information in the minimum amount of time and at a greatly reduced cost. The methodology also enables standardization of comparisons of the key characteristics of similar fabrication processes.

An example of NBTI extraction and processing for a small geometry process is presented.

Keywords—process qualification; reliability; NBTI; HCI

I. INTRODUCTION

The purpose of this paper is to provide information on ProChek™, the comprehensive process mismatch and reliability characterization tool for advanced transistor technologies.

II. NANO-GEOMETRY CMOS RELIABILITY CHALLENGES

Increasing circuit performance demands access to advanced semiconductor fabrication processes, yet reliability and schedule requirements create obstacles to using these increasingly complex technologies. Successful technology insertion requires knowledge of failure mechanisms, design limitations and screening flow.

Modern nano-geometry CMOS circuits have numerous reliability concerns that have to be accounted for during design and verification cycles. The circuits age during the operational life due to effects such as negative and positive bias temperature instabilities (NBTI, PBTI), time-dependent dielectric breakdown (TDDB), stress-induced leakage current (SILC), hot carrier injection (HCI), electromigration (EM), and stress migration (SM). The varying temperature extremes experienced by circuitry during the operation also affect overall reliability. As an example, the lifetime of transistors in a 65 nm CMOS technology was found to be only 0.2 years due to hot carrier injection when biased at a constant voltage bias condition [1]. It is obvious that comprehensive characterization of degradation effects is needed during the design phase of modern nanotechnology microelectronics circuits.

III. PROCHEK RELIABILITY CHARACTERIZATION INSTRUMENT

Ridgetop Group provides a solution to this problem by providing an easily portable reliability testing platform that can be used as the standard test method by any IC design team.

Ridgetop has designed a portable and user-programmable process reliability evaluation system (ProChek™) for CMOS and BiCMOS fabrication processes. The system can be used for accurate yet rapid and cost-effective qualification of the intrinsic reliability of CMOS and BiCMOS processes (including SiGe processes). The method uses a **Test Coupon** that is fabricated in multiproject wafer (MPW) shuttle runs in order to minimize the costs and expedite the qualification phase. The reliability qualification is performed using measurement and data collection circuits inside the **Benchtop Tester** instrument. The **Test Card** is a simple interface card that holds the Test Coupon. The Benchtop Tester is controlled by a **Host Controller**, which is a user-invoked graphical user interface (GUI) software application on a PC. The Benchtop Tester and the Host Controller software are universal and can be used with Test Coupons from different fabrication runs. The Test Coupon is standardized, all-digital structure and can be ported to different fabrication processes with minimum engineering cost.

This instrument eliminates the need for expensive test equipment in fabrication process reliability characterization, and it simultaneously provides a standardized platform for IC designers to perform the required reliability tests.

The four components of ProChek are shown in Fig. 1.

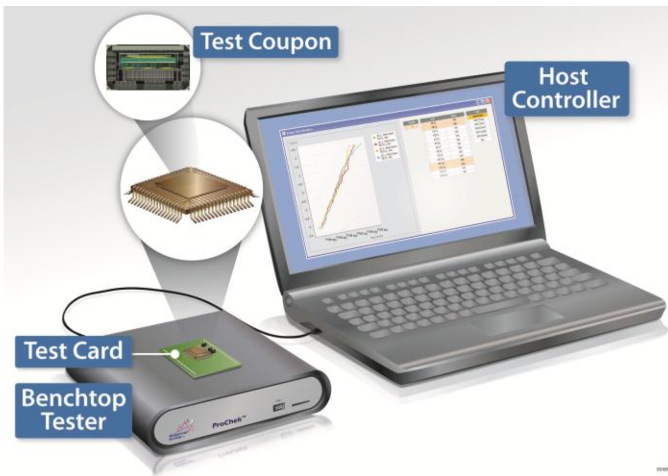

Fig. 1. ProChek test system

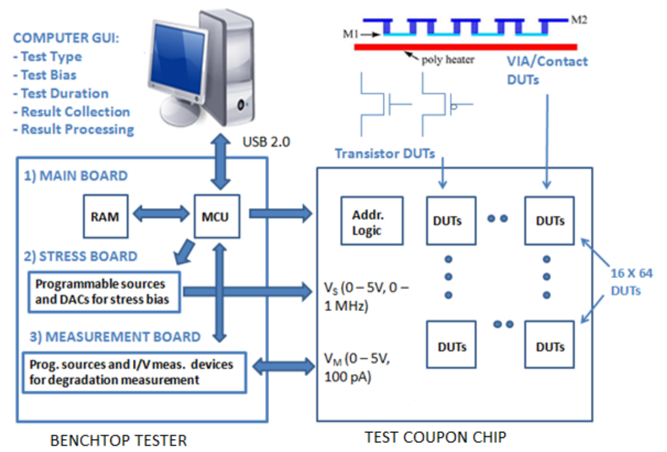

Fig. 2. Structure of ProChek

In addition to the four-component structure shown in Fig. 1, Ridgetop's ProChek supports a test flow in which customers can use their own test equipment instead of using the Benchtop Tester. Ridgetop can provide the test structure IP and the result characterization software.

The silicon area consumed by the test structure IP (Test Coupon) can be made smaller or larger, depending on the customers' requirements. The test structure block can even be made small enough (e.g., 300 µm X 300 µm) to easily fit on the same die with the actual IC and it can then be used for reliability characterization of that die.

ProChek provides everything needed for fabrication process characterization for modern advanced transistor technologies. Moreover, if a tight development schedule puts constraints on the process characterization, all of the work can be outsourced to Ridgetop engineers.

A. Details of ProChek

Fig. 2 is a more detailed illustration of Ridgetop's fabrication process reliability evaluation system (ProChek) which includes: Host Controller, which is a GUI application on a PC; Benchtop Tester, which consists of the main printed circuit board (PCB) and two daughterboards (these three boards are named MAIN BOARD, STRESS BOARD and MEASUREMENT BOARD); and Test Coupon, which is a packaged silicon chip with arrays of test structures and which is placed on the Test Card. By using the GUI, the test structures can be programmed to be subjected to highly accelerated test conditions that target all critical failure mechanisms that are concerns (TDDB, NBTI, etc.). Fabricated Test Cards and the Host Controller software are universal and can be used with Test Coupons from different fabrication runs.

1) Benchtop Tester

The reliability qualification is performed using measurement and data collection circuits on a common PCB board (named MAIN BOARD in Fig. 2) inside the Benchtop Tester enclosure, which holds two daughterboards (named STRESS BOARD and MEASUREMENT BOARD in Fig. 2). These two daughterboards are used to perform the highly accelerated stressing and the degradation measurement functions, and they contain carefully selected commercial off-the-shelf (COTS) parts, such as programmable voltage sources and digital-to-analog converters (DACs); and Ridgetop's proprietary low-noise current monitors. The voltage measurement capability on the MEASUREMENT BOARD provides 500 ns measurement time and <5 µV accuracy, whereas the measurement time for the low current measurements is 10 µs with 3 pA accuracy and excellent repeatability.

One of the main advantages of Ridgetop's ProChek system is highly parallelized testing. Up to 1,000 DUTs (devices under test) can be subjected to a test simultaneously.

Note that Ridgetop's ProChek is designed for "highly parallelized package-level tests," but can be used with wafer and die-level test setups as well.

2) Host Controller

The whole test system is controlled from the Host Controller, which is a software application on a PC. From the user interface (GUI), the user can program test bias magnitudes and waveforms; test temperatures; and test durations. The GUI also collects the measurement results and processes them for better visibility of the failure effects. For example, the GUI has an algorithm that calculates threshold voltage (V_T) shifts from drain current measurements. The GUI contains a rich suite of built-in reliability test templates that target most known degradation mechanisms. Fig. 3 shows a snapshot of the built-in "charge to breakdown" (QBD) test template inside the ProChek GUI.

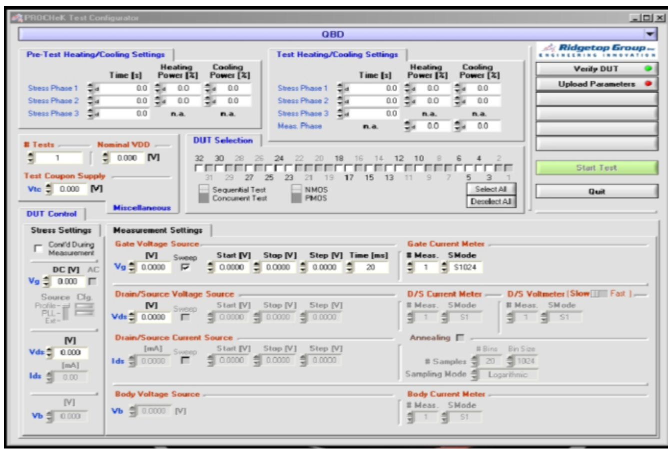

Fig. 3. This particular template inside the ProChek GUI is used to control "charge to breakdown" (QBD) gate oxide integrity tests

3) Test Coupon

Ridgetop's proprietary ProChek test structure IP (i.e., the Test Coupon) contains arrays of programmable test structures, as seen in Fig. 2. The Test Coupon is a 1 mm X 1 mm chip that is fabricated on a multiproject wafer (MPW) run and packaged in order to minimize the test costs and expedite the qualification phase. Ridgetop has selected an optimal high-reliability ceramic package for the Test Coupon. The current version of the Test Coupon has 6 arrays of 32 DUTs, and Test Coupons with more or fewer DUTs can be fabricated, if requested. Note that Test Coupons with fewer DUTs have a smaller layout area. Ridgetop has approximated that the minimum achievable silicon area that fits the Test Coupon, including all the required bonding pads, address logic, and few hundred DUTs is 500 µm X 500 µm, when fabricated in a 45 nm CMOS process.

The Test Coupon is a standardized, all-digital architecture and can be ported to many different fabrication processes with minimum engineering cost. All of the control logic in the Test Coupon design can be synthesized from VHDL code and the DUTs are easily portable library files. The DUTS on the Test Coupon include: NMOS, PMOS and I/O transistors (different sizes); via and contact test structures; small circuits, such as ring-oscillators; and radiation effect test structures. Note that even if the Test Coupon has been designed to contain only easily portable digital logic, it can be used to characterize reliability problems that are concerns in both digital and analog circuits.

a) Test Strustures for Failure Effects

Highly accelerated stress tests targeting reliability concerns, such as negative bias temperature instability (NBTI), time-dependent dielectric breakdown (TDDB), stress-induced leakage current (SILC), hot carrier (HC) damage, electromigration (EM), and stress migration (SM) can be performed with ProChek. The degradation is significantly accelerated with the combination of stress voltages that are higher than VDD and high temperatures, created with localized, on-chip polyresistor heating elements. The tightly controlled heating capability can also be used to characterize the effect of varying operating temperatures on circuit reliability, which is of interest to engineers of modern high-density systems.

Both DC and AC stress bias conditions can be programmed on the test units, which allows making accurate approximations of circuit lifetimes in realistic operation conditions. Note that in this reliability engineering context, DC and AC biases mean constant voltage bias and varying voltage bias, respectively.

The ProChek system can also be used to evaluate the interactions between various aging effects, which may have unpredictable effects on circuit parameters.

The aging of individual transistors is dependent on the exact bias conditions it experiences during the operation, as well as global conditions such as temperature, which can have a significant gradient across the die. The transistor parameters also have a statistical variance due to process mismatches. Interestingly, the degradation of individual transistors also has a statistical variance of its own; i.e., two identical transistors under the exact same bias conditions and temperature will age differently. ProChek captures both effects: the variance due to process mismatches and the variance in different aging mechanisms, such as NBTI. Traditionally, the measurements needed to capture the statistical variation in aging processes are lengthy and expensive. Moreover, even if these data are measured by the manufacturer, only a limited amount of these data are made available outside the foundry.

The Test Coupon in ProChek includes large sample sizes of test structures and thus provides very good statistical models for the physical effects that can be used as the basis of accurate aging simulation models.

To our best knowledge, there are no other solutions currently available for rapid, low-cost reliability testing and aging parameter capture targeting nanotechnology ICs. Certainly, none that are commercially available.

b) Acceleration of Circuit Degradation with Localized On-Chip Heating Elements

Concurrently, comprehensive reliability characterization work is very time-consuming and costly, partly due to the fact that the degradation mechanisms cannot be accelerated enough with the traditional methods. ProChek has innovative local heating elements that will shorten the test times by orders of magnitude, allowing very comprehensive evaluation within reasonable time and budget limits. The on-chip, tightly controlled heating capability can also be used to characterize the effect of varying operating temperatures on circuit reliability, which is of interest to the engineers of modern high-density systems.

A simplified illustration of a heating structure used for accelerating the electromigration and stress migration degradation in vias is shown in Fig. 4 a), and typical electromigration-induced voiding around a via is shown in Fig. 4 b). Snapshots from thermal simulations on similar local heating structures that are around PMOS transistors are shown in Fig. 5 a) and b). Fig. 5 a) shows two blocks of 64 PMOS transistor DUTs under localized heat on a packaged and actively cooled Test Coupon chip. Temperature drops quite abruptly from 322 to 22 °C on the chip, which proves that the

neighboring unstressed test structures do not undergo any degradation, and that the chip package will not be damaged even if local temperatures above 300 °C are used. Fig. 5 b) is a zoomed-in view showing the U-shaped heaters around the stressed transistors.

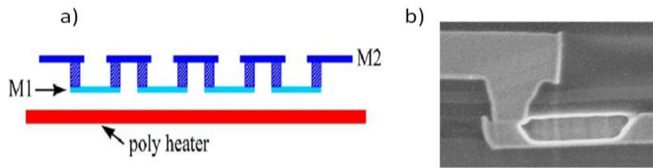

Fig. 4. a) Local poly-silicon heater can be used to accelerate the degradation mechanisms in vias; b) typical electromigration-induced void in the vicinity of a via [2]

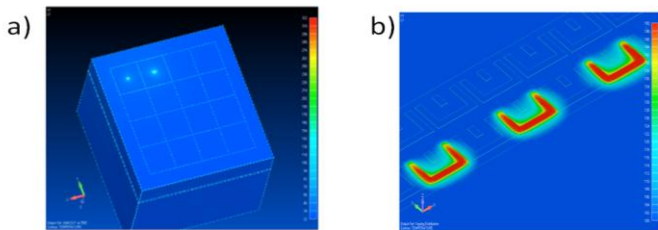

Fig. 5. a) Two blocks of 64 PMOS transistor DUTs under localized heat on an actively cooled packaged Test Coupon chip, b) zoomed-in view showing the U-shaped heaters around the stressed transistors

Similar local heating elements are commonly used in fast wafer level reliability testing (fWLR). Reported data from fWLR tests show that every 50 °C increase in the stress temperature will reduce the total test time by one order of magnitude in electromigration tests [2]. Similar data have been reported for NBTI. This means that Ridgetop's local heating structures that can be used to heat the DUTs up to 325 °C will shorten the required test times by several orders of magnitude compared to room temperature tests. This will allow comprehensive process characterization within reasonable time and budget limits.

Note that the user can set any stress temperatures between 25 and 325 °C from the GUI. Using the developed heating mechanism to significantly accelerate the aging is optional.

IV. ProChek Development Schedule

Test Coupons have been fabricated on seven different CMOS and SiGe fabrication processes so far, ranging from 45 nm node to 180 nm node. The test system has been used to characterize these processes.

Fig. 6 shows typical test results from a ProChek reliability test. In this test 16 transistors were subjected to hot carrier stress

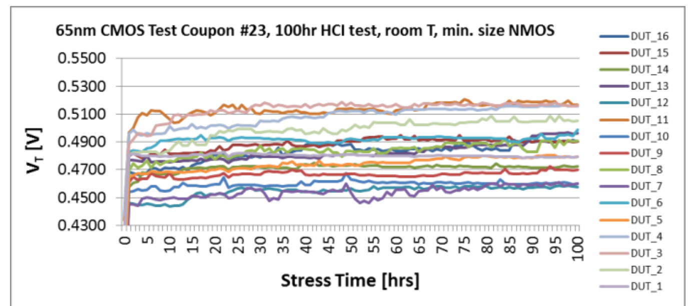

Fig. 6. Hot carrier injection (HCI) test results obtained with the ProChek test system

V. Summary

The decreasing reliability of the newest nano-geometry CMOS fabrication processes is a critical problem. Ridgetop's ProChek can be used for accurate, rapid and low-cost fabrication process reliability characterization as a part of the IC design and qualification cycles. Providing an easy-to-use GUI with data processing capabilities, universal benchtop test instrument, and portable test chip IP, ProChek can be used as the standard reliability evaluation system among IC engineers.

References

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