RGSJBIST

PRODUCT BRIEF

Ridgetop Group Inc

ENGINEERING INNOVATION

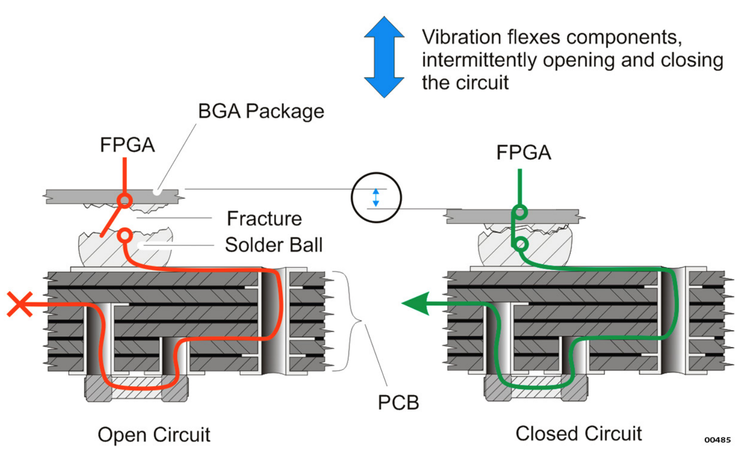
SJ BIST™ for Custom Applications

Advanced Electronic Interconnect Diagnostics/Prognostics

The Interconnection Prognostic Solution

- Built-in self-test (BIST) intellectual property (IP) detects damage to sensitive electronic and electrical interconnects
- Applications include monitoring and detection of degradation and faults in internal IC interconnects, substrates, packages, boards, and wires
- Supports interconnect reliability test and qualification
- Improves fault coverage without significantly increasing complexity of system
- Improves fault coverage for advanced redundancy management without using redundancy techniques
- Provides positive correlation of hardware faults to intermittencies

Interconnects in today's complex integrated circuits (ICs), electronic boards, and systems are subject to subtle damage and degradation that can affect device performance and reliability and ultimately cause the device to fail. The initial damage may occur during the manufacturing and assembly process or after the ICs, boards, or systems are deployed in the field. Faults may arise from out-of-calibration manufacturing equipment, impurities in bonding materials, environmental stresses, weak connections, or random process fluctuations. Whatever the cause, detecting interconnection faults before they progress sufficiently to cause catastrophic failure is both difficult and essential.



How intermittencies occur in an FPGA in a BGA package

Some problems have become particularly acute with today's advanced manufacturing technologies. For example, IC die have become so thin that small silicon substrate cracks occur frequently during initial manufacture and packaging, and these weak die may go undetected until the cracks are subsequently aggravated by handling, vibration, or temperature anomalies. In a similar way, the complex interconnect structures within packages are sensitive to weaknesses that may go undetected during the testing process but can cause device and system failure during subsequent handling and application. Similarly, board assemblies involving IC packages with hundreds or even thousands of connections to the underlying printed circuit board (PCB) may have weak solder joints that are not bad enough to fail manufacturing tests, but fail during use in their end applications.

Prior to the development of Ridgetop's Solder Joint Built-in Self-Test™ (SJ BIST) solution, there were no commercially viable methods for detecting interconnect-related intermittencies and high-resistance defects in functioning ICs, packages, and PCB assemblies. SJ BIST is an in situ monitor designed to continuously monitor and detect static and dynamic occurrences of interconnect resistance increases and ruptures, and then alert the system regarding the condition of interconnects and their assembly points such as solder joints, bond wires, and cabling. Devices with weak interconnects may be screened and discarded during manufacturing and test phases.

Maintenance is also facilitated by constant monitoring, either through replacement or by switching to a redundant system prior to catastrophic failure. In addition to solder joint health monitoring, SJ BIST serves a wide range of applications where interconnect integrity and reliability are of concern.

Thermal stress and physical stress are primary causes of interconnect fatigue damage. Thermal-related damage results from differences in the coefficients of thermal expansion of the materials in the IC package, solder, wiring, interconnections, and PCB, as well as from heating and cooling due to ambient temperature changes and power on-off cycling.

The damaged interconnects typically manifest themselves by intermittent increases (spikes) in the resistance of the network from milliohms to tens of ohms or more, and medium- to high-resistance spikes of increasing frequency and duration. As interconnect faults tend to be initially intermittent in nature, they are difficult to diagnose. Often, when a removed component, assembly, or board is examined and bench-tested, "No Trouble Found" (NTF) is the diagnosed code.

SJ BIST enables early detection and identification of a device or assembly likely to experience a malfunction. The prognostic is programmed/designed into the host circuit and an (optional) small capacitor is attached to a loop formed by one or more pairs of functionally unused driver/receiver pairs, which are monitored or tested by SJ BIST. Because a synthesizable hardware description of the SJ BIST functional IP is available expressed in Hardware Definition Languages (HDLs) such as Verilog or VHDL, it is easily inserted, synthesized, and implemented inside any programmable or hard-coded IC.

The only IC real estate overhead required for an SJ BIST core consists of a small number of logic gates, one or more dedicated signal paths through the portions of the circuit to be monitored (e.g., through the substrate, package, and/or board), and a status/control connection. Interfacing with common communication structures (such as SPI or I2C) or commonly used test infrastructure such as IJTAG is an option. An SJ BIST instance requires less than 100 equivalent gates. The actual gate count depends on the desired monitoring, recording, and notification capabilities. A typical application comprises several block instantiations, each monitoring critical circuit locations and features.

While a particular damaged interconnect trace, wire, bond, or cable might not result in immediate operational failure of the host circuit, the damage indicates that the host circuit is no longer reliable. The occurrence of even a single fault is a prognostic warning; to avoid a near-term operational intermittent or long-lasting fault, maintenance or other mitigation is required. The early detection made possible by SJ BIST enables corrective actions using condition-based maintenance (CBM) procedures to be performed, thus avoiding operational failures.

In addition to prognostics, SJ BIST can be used in newly designed manufacturing reliability tests to investigate failure modes related to the host circuit package or assembly and other interconnect reliability issues.

SJ BIST is part of the Sentinel Interconnect™ product line, a member of the Sentinel Suite™ family of solutions.

Applications

Applications include monitoring and detection of:

- Defective or degraded board-to-package solder joints for BGA and other high pin-count packages
- IC die cracks
- Internal delamination between IC layers
- Defective or degraded through-silicon vias (TSVs) in stacked die packages
- Package qualification
- Cabling and board-to-board connectors
- Soldering/assembly process qualification

Customer Testimonial

"SJ BIST is the first known direct in-situ measurement that is a true canary for intermittent electrical contact between bumps, PCB, and package." — *German Automotive Firm*

Need modified or custom design? Contact Ridgetop at +1 520-742-3300 to discuss your ideal solution!

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