
# *Interconnect Intermittency Detection with SJ BIST™*

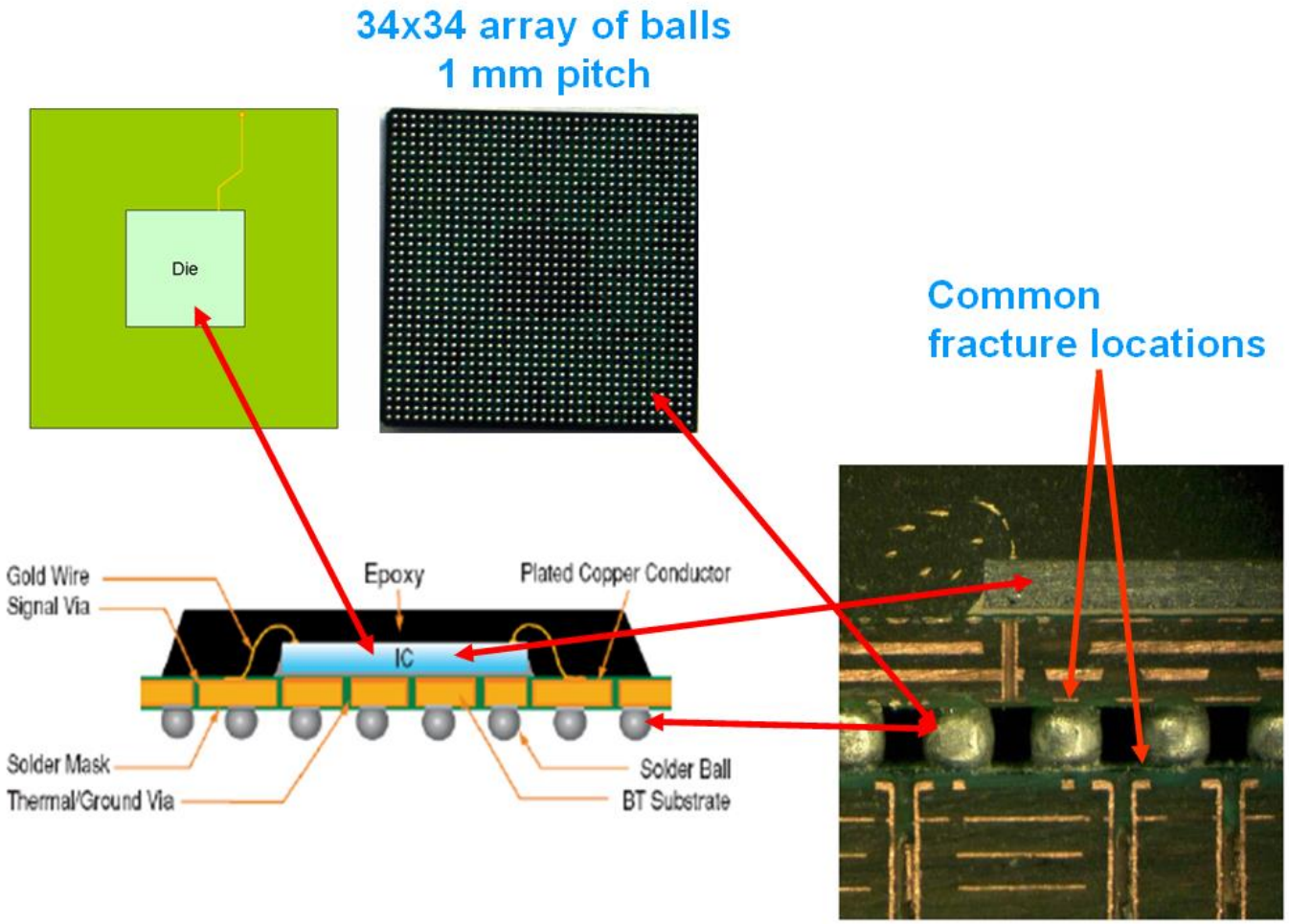
# Agenda

- What is SJ BIST?
- Interconnect Reliability – Background
- SJ BIST Basics
- SJ BIST Operation
- SJ BIST Application
- Summary & Conclusions

# What is SJ BIST?

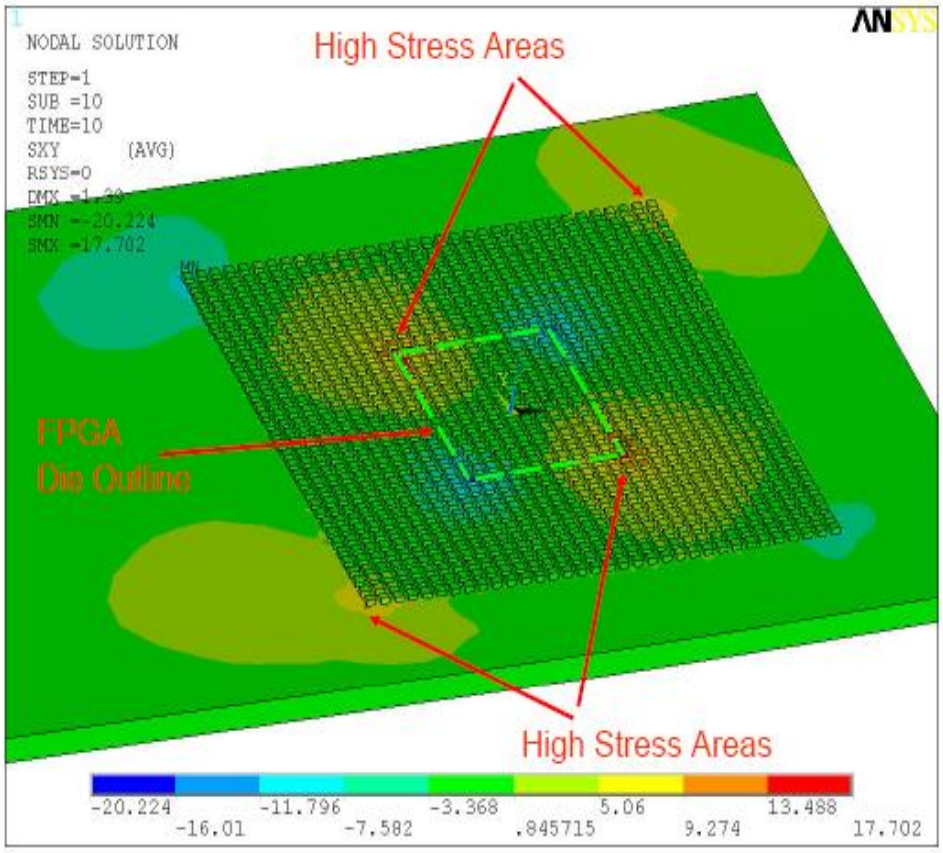
- SJ BIST = Solder Joint Built-in Self-Test
  - Original solution enabling the verification and validation of solder joint interconnect reliability
  - Originally developed for FPGA-BGA applications
  - Can be applied to validate the integrity and reliability of any type of interconnection

# BGA – PCB Relationship: Die, package, wiring, pins

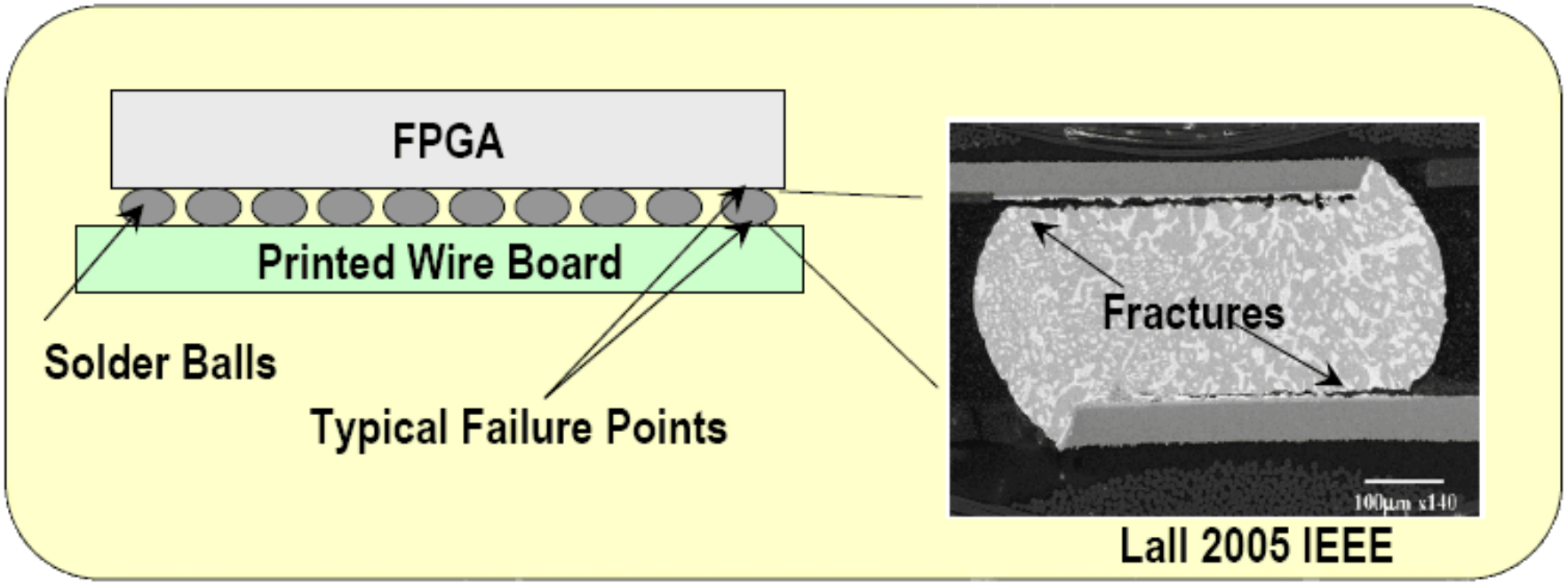


# Defects: Location of Cracks/Fractures

- Corner pins likely to fail first
  - High stress areas, and corners of the BGA package and die

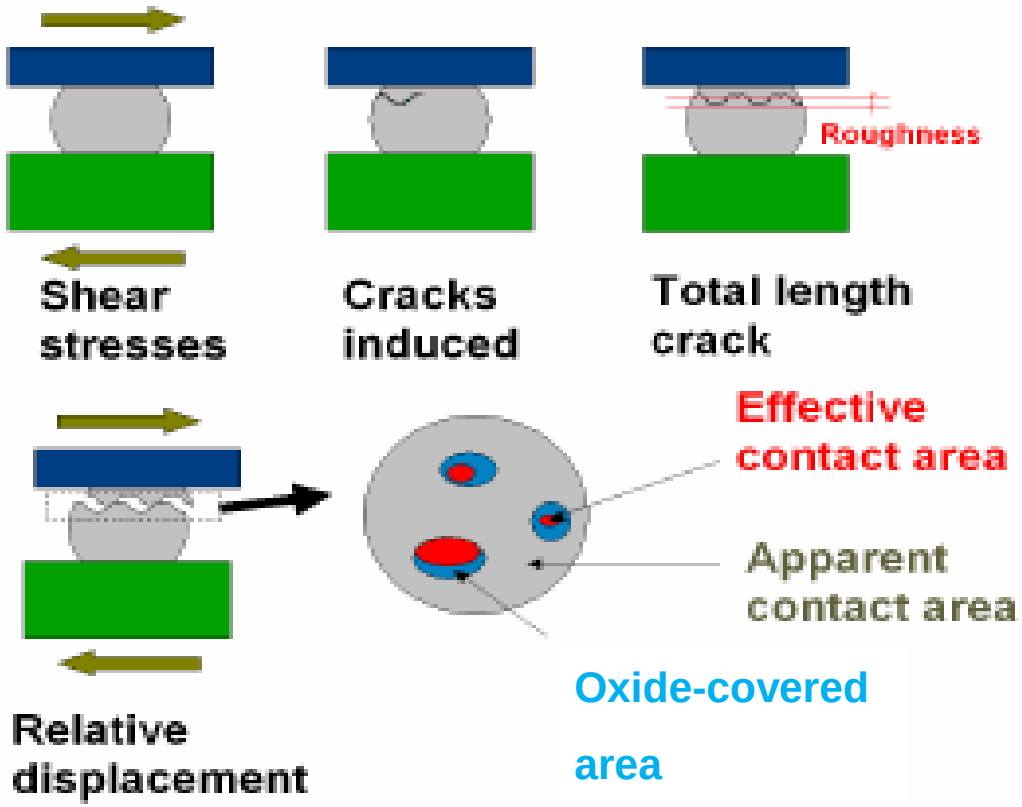


# Solder Balls, Cracks and Fractures



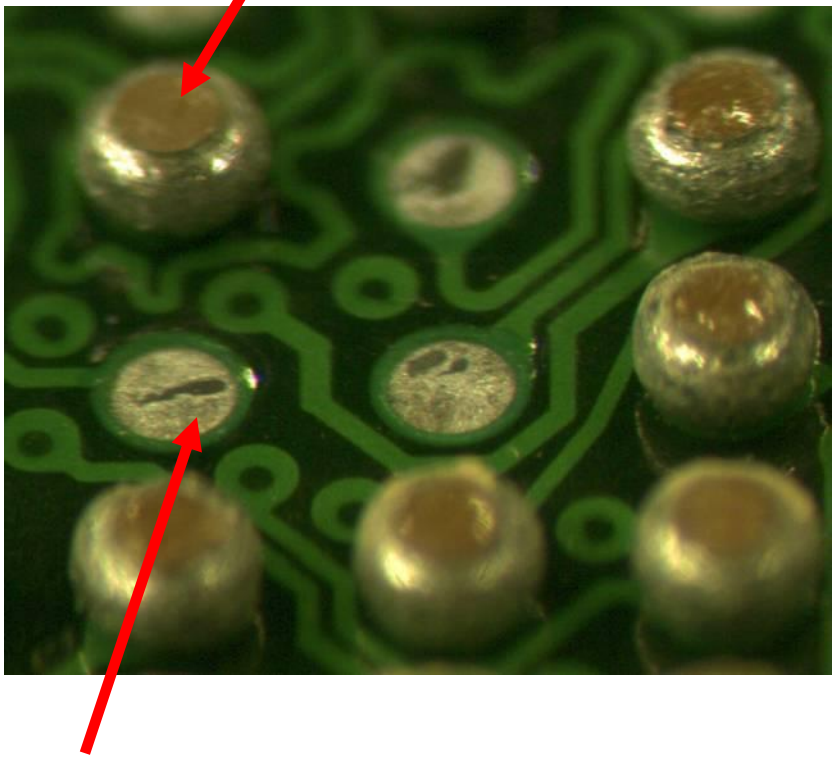
# Mechanisms of Failure

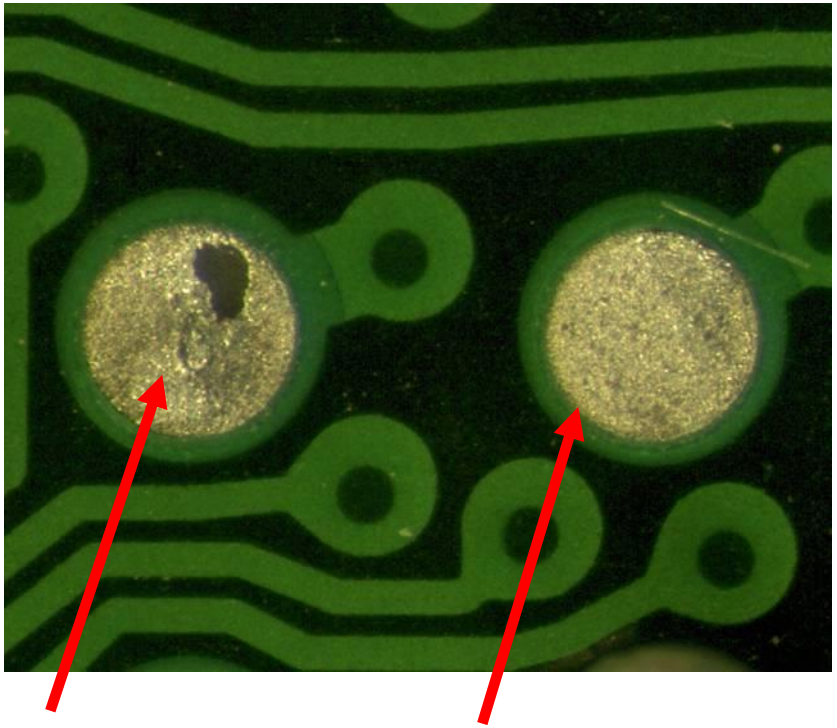
- Fatigue fractures (cracks) are caused by thermo-mechanical stress/strain
- During periods of high stress, fractured bumps tend to momentarily open and cause intermittent faults of high resistance for periods of ns to µs
- Over time, contamination and oxidation films occur on the fractured faces: the effective contact area becomes smaller and smaller
- Transient opens can be detected by event detectors



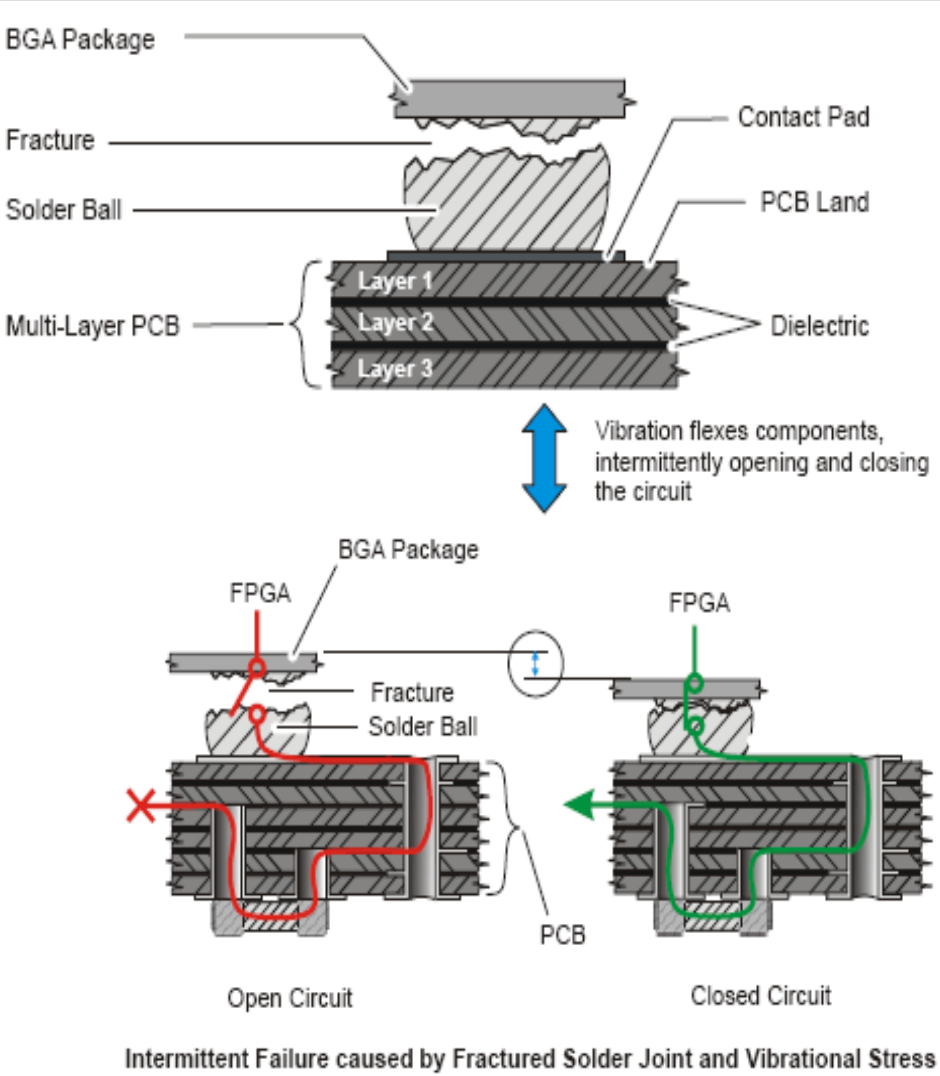
# Mechanics of Failure

## HALT results - Pulled FPGA – Damaged Solder Balls



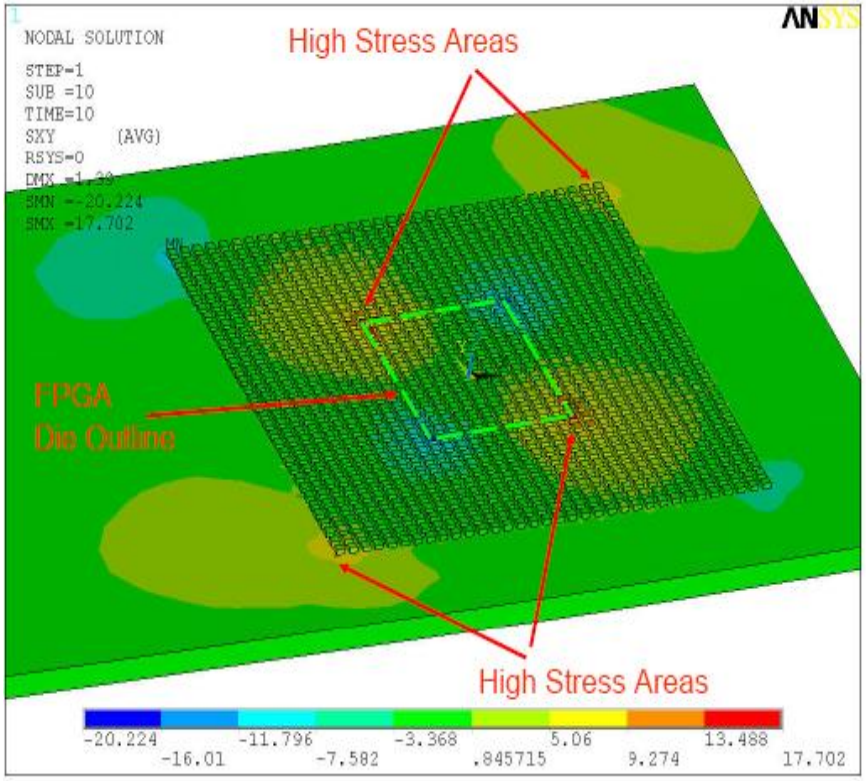



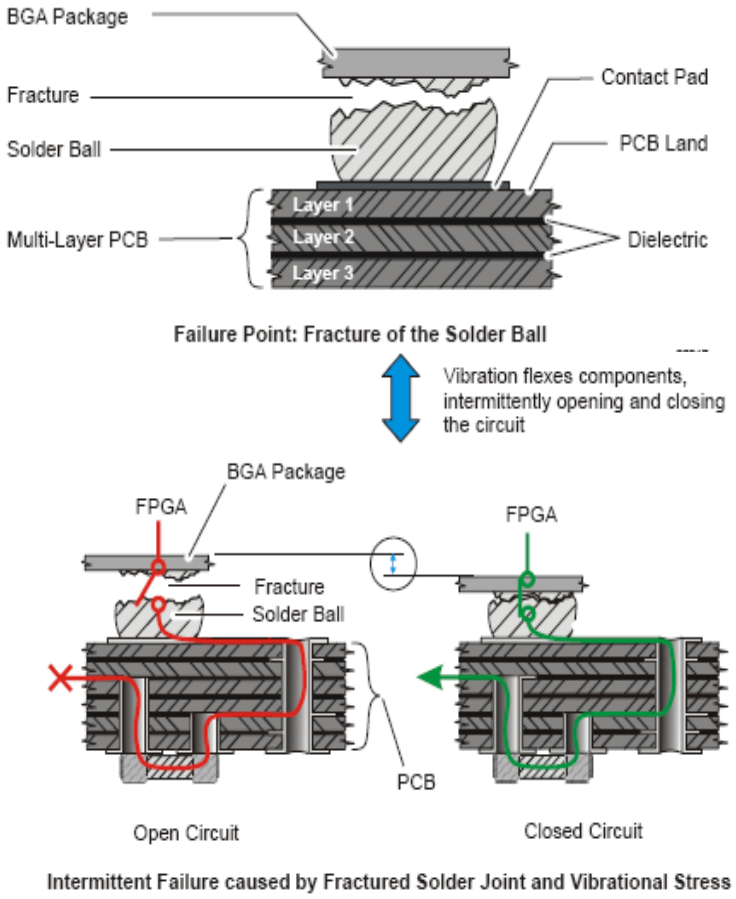
# Fractures and Intermittency




Intermittent Failure caused by Fractured Solder Joint and Vibrational Stress

# Defects: Fractures & Intermittency

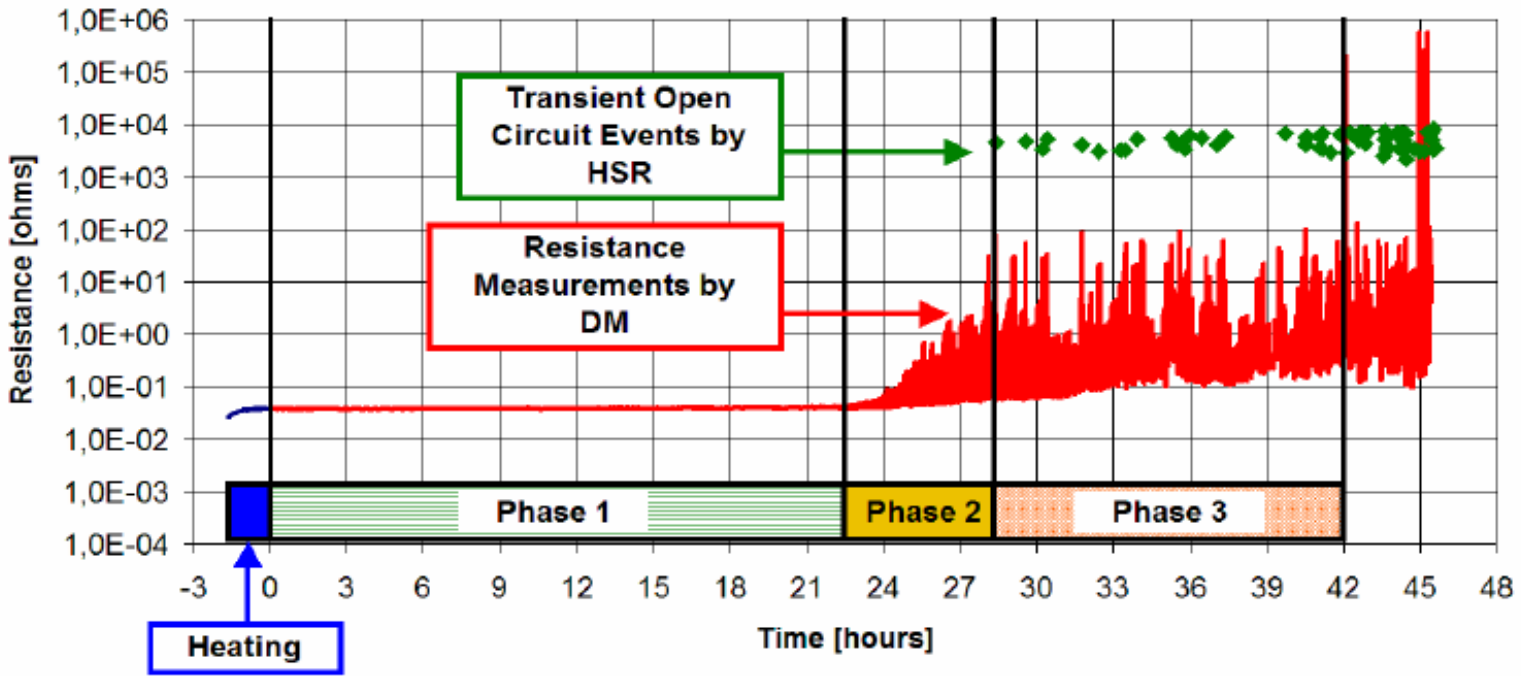



**Intermittent Failure caused by Fractured Solder Joint and Vibrational Stress**

# Intermittent Faults

- Faults are intermittent: confirmed by CAVE, Auburn Univ., German automobile manufacturer, BAE Systems and other firms
  - **Occur during periods of increasing strain**
  - **Multiple occurrences per cycle**
  - **Industry standard: 200 ohms +, 200 ns +**



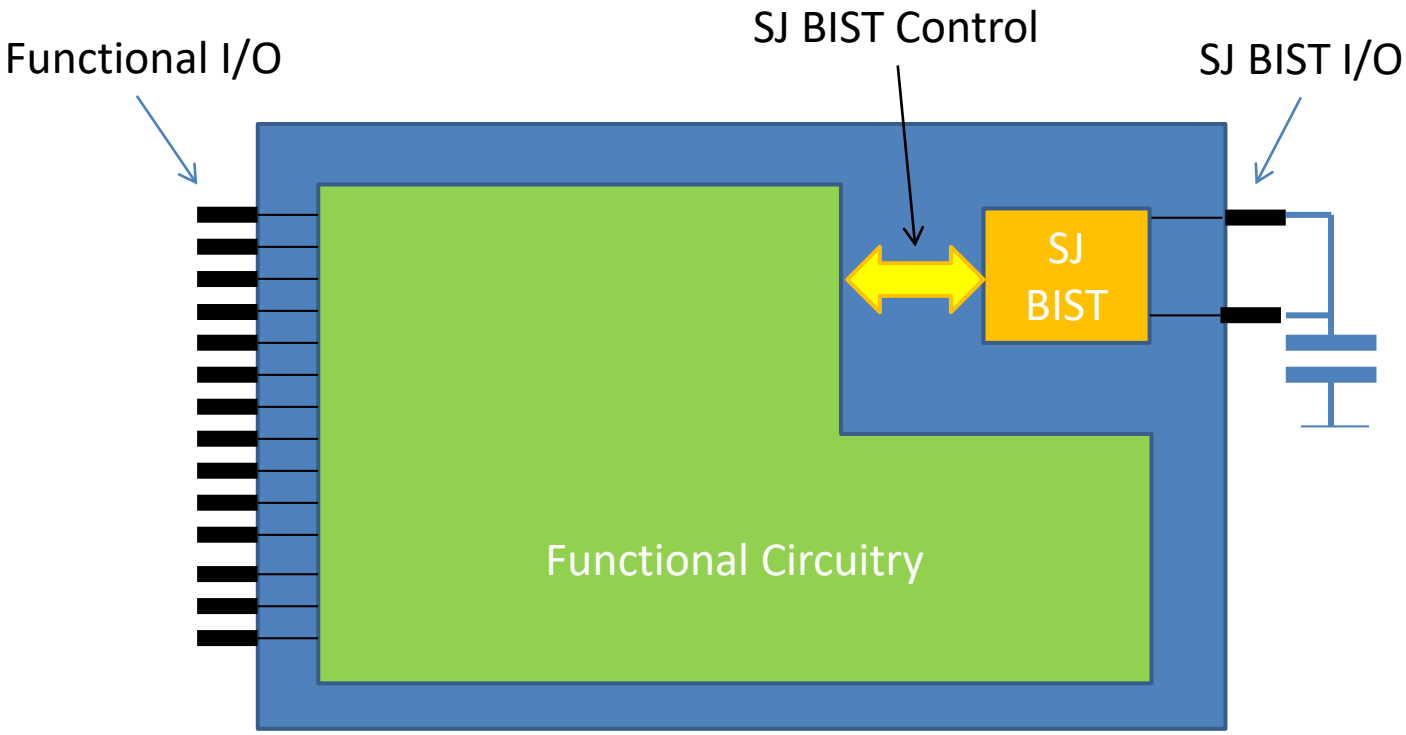
# Intermittencies

- With present technology, reported electronic system problems in the field cannot be duplicated at the service point or in the lab
- "Three/Four-letter" words (CND, NTF, RTOK)
  - Could Not Duplicate (CND)
  - No Trouble Found (NTF)
  - Retest OK (RTOK)
- 50 to 80% of these CND/NTF/RTOK problem categories are reported by service personnel.
- Major culprits – Solder joint intermittencies and NBTI effects in deep submicron ICs

# SJ BIST Objectives & Features

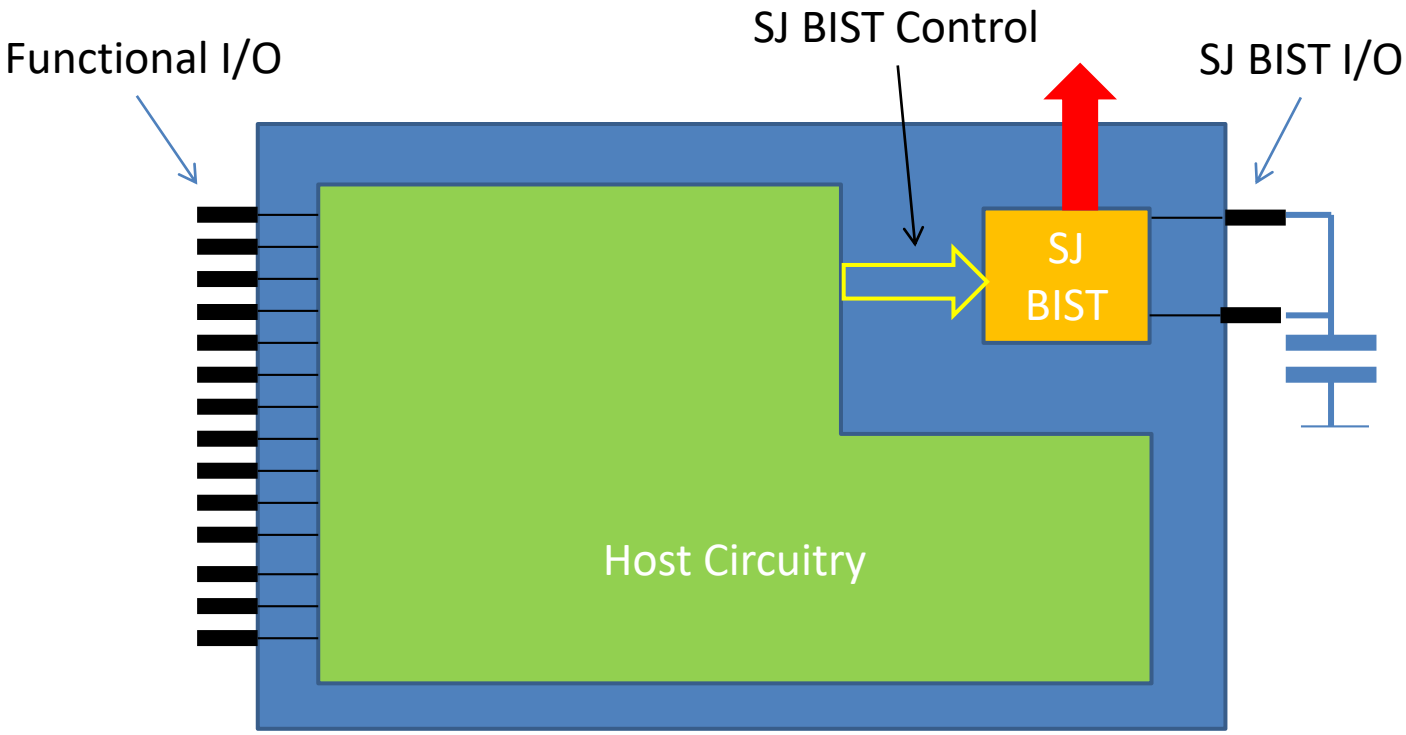
- Objectives
  - Detection of impending interconnect failures
  - Unique in-situ testing in operating circuits
  - Technology-independent
- Feature and Benefits
  - Detects ball fractures prior to catastrophic failure of circuit
  - Provides actionable maintenance data
  - Independently tested and verified
  - Endorsed by leading automotive and aerospace customers

# SJ BIST Implementation




- SJ BIST runs concurrently with host circuit
- SJ BIST requires dedicated I/0

# SJ BIST Implementation

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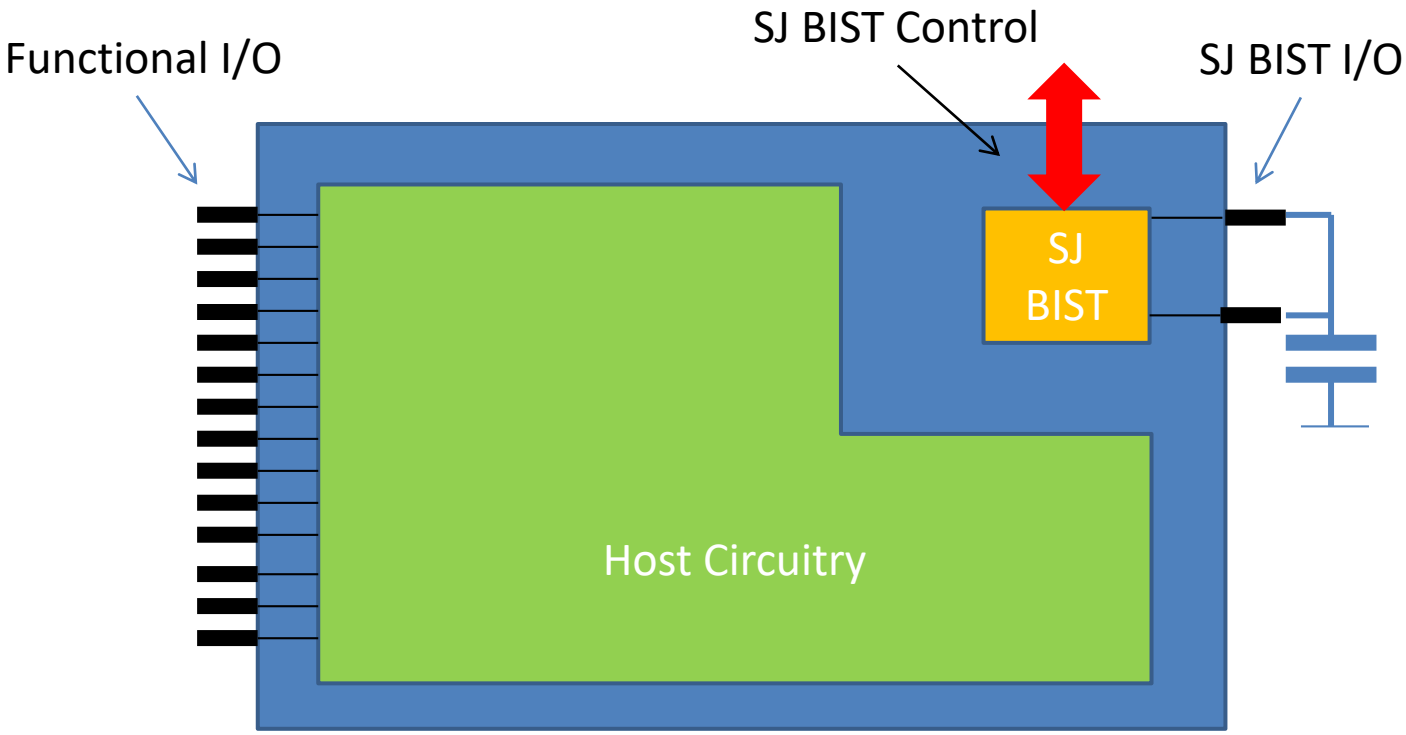
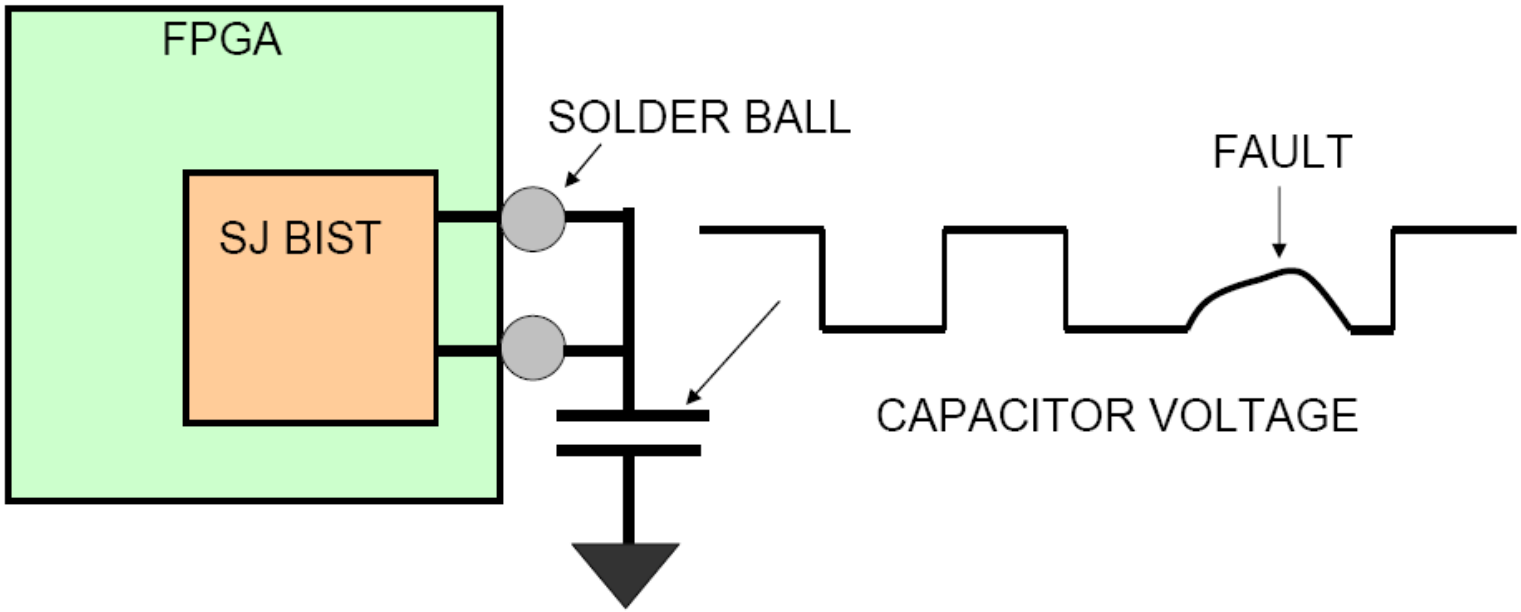



- SJ BIST runs concurrently with host circuit
- SJ BIST requires dedicated I/0

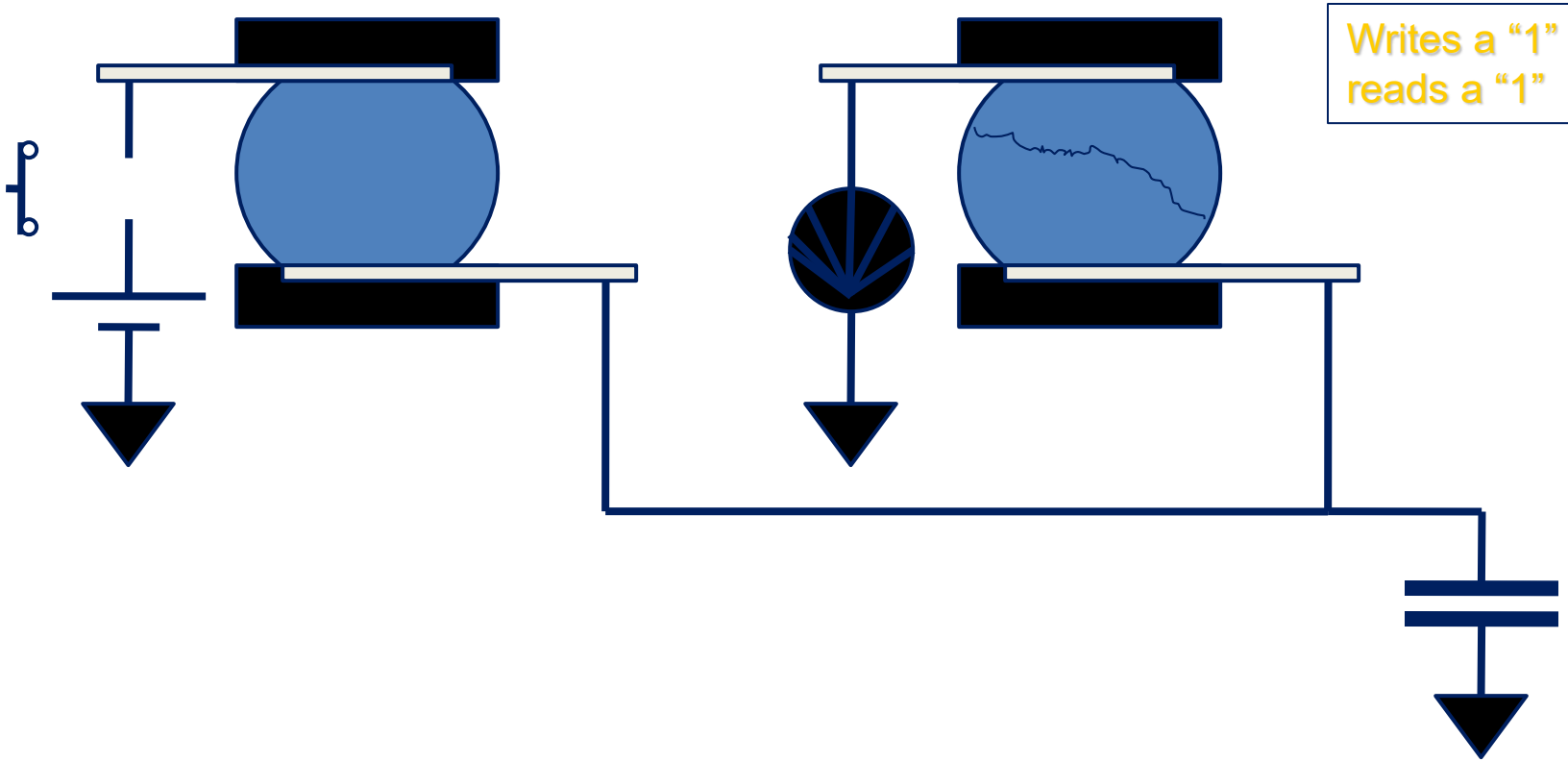
# SJ BIST™ Operation

- Similar to a simple memory test: W0 – R0; W1 – R1
- Runs concurrently with host circuit
- Verilog/VHDL core (patent pending)
  - Each core tests two I/O pins
  - Pins are externally wired together
  - Small capacitor connected to the two pins



# SJ BIST Operation

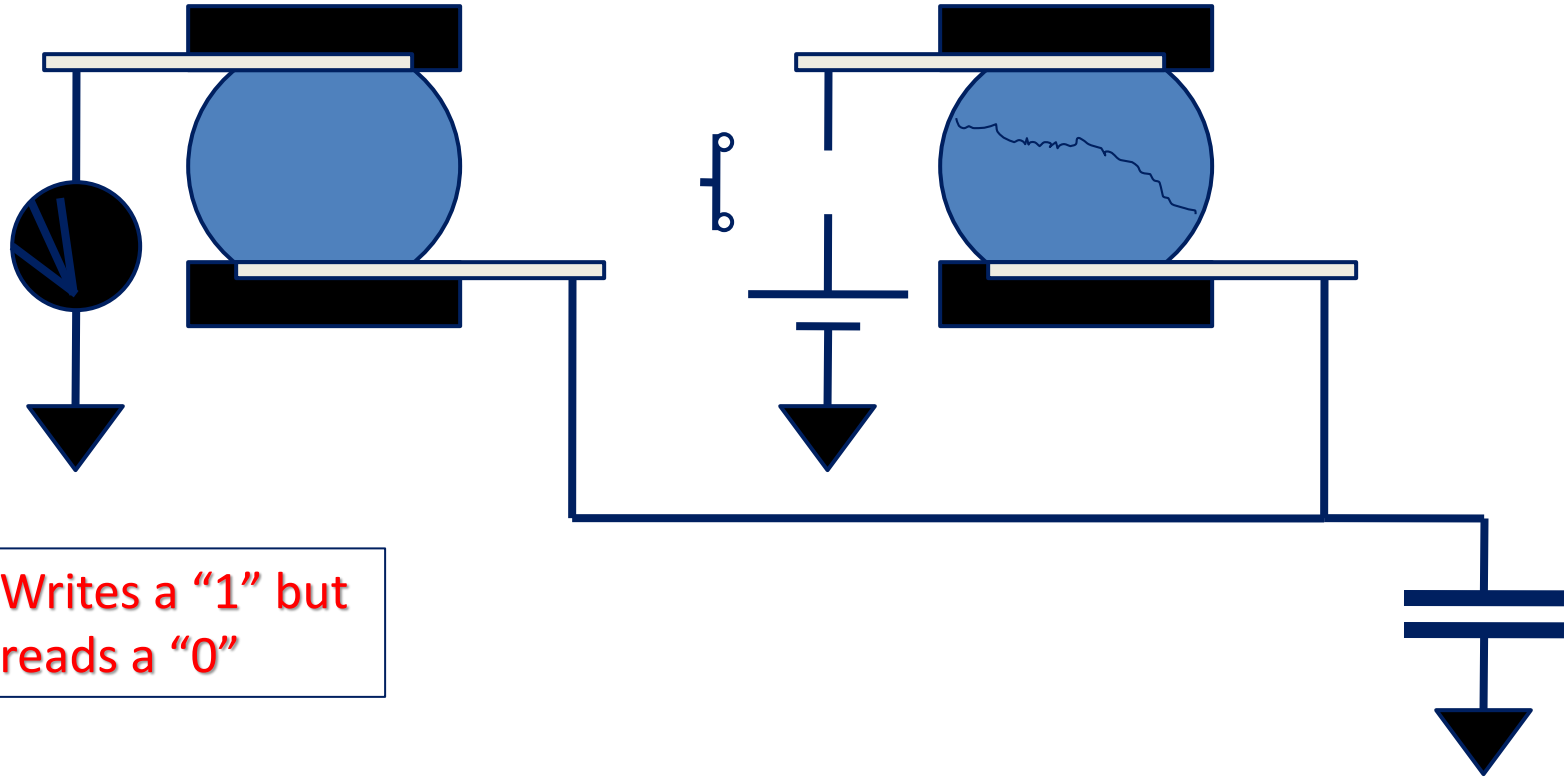
## Healthy Solder Joint



Writes a “1” and reads a “1”

# SJ BIST Operation

## Faulty Solder Joint



Writes a “1” but reads a “0”

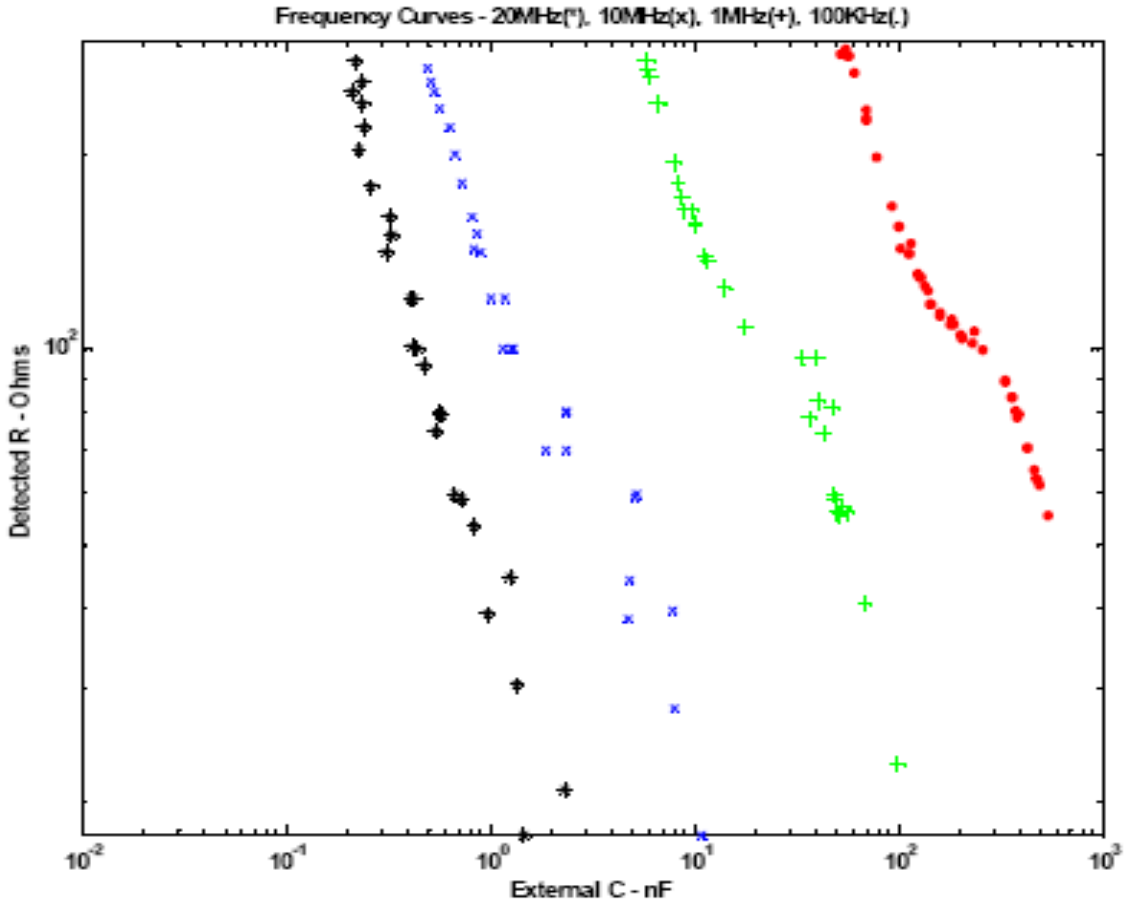
# SJ BIST Capacitor

- Function of operating frequency & desired sensitivity

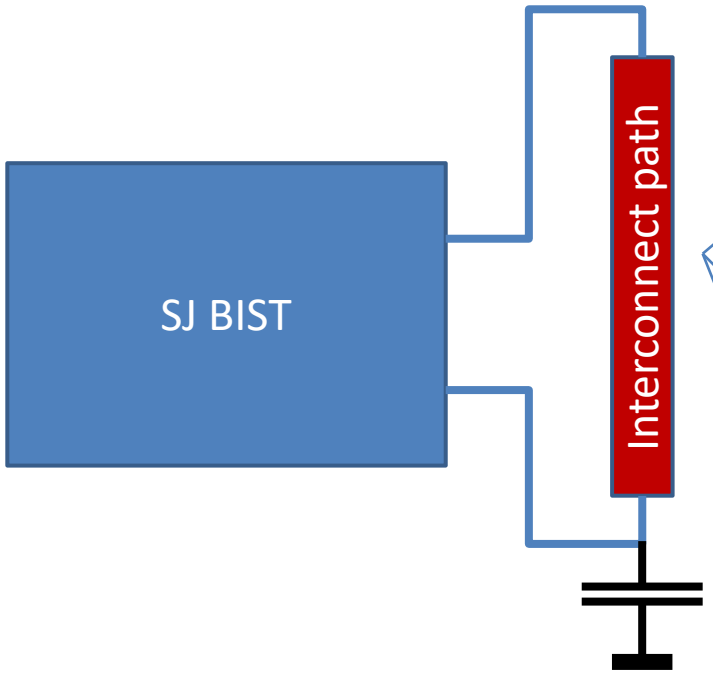
300 Ohm

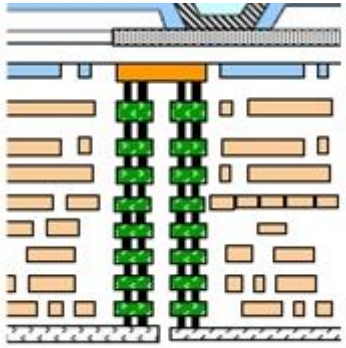
100 Ohm

10 Ohm

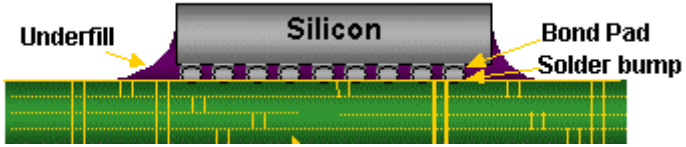


# SJ BIST Application

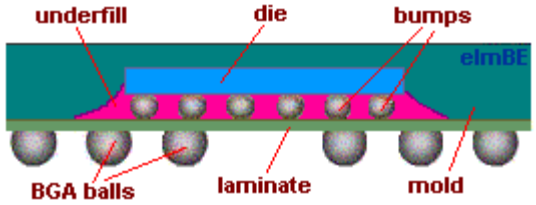


On-chip interconnects




Die to substrate (incl. bumps)

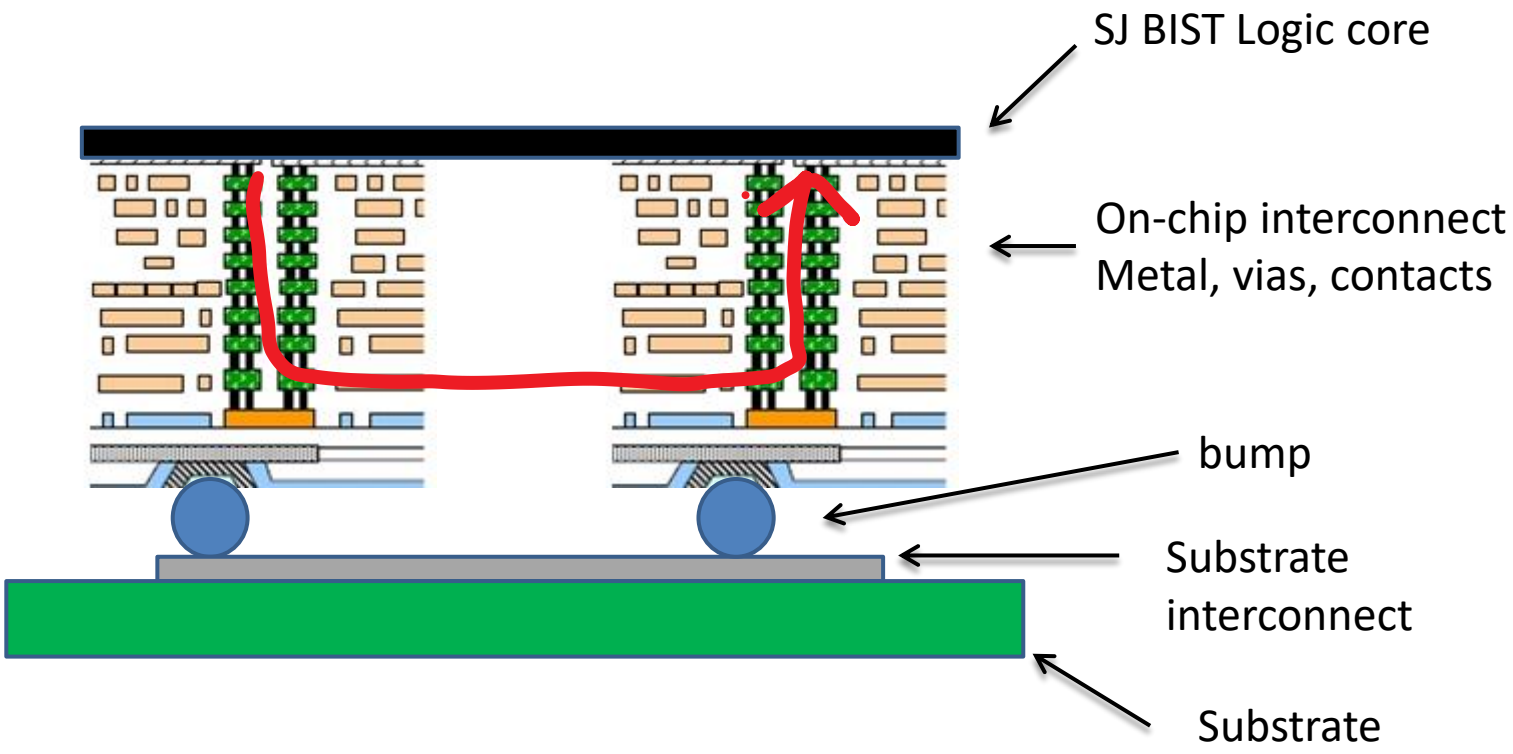



Die to board (incl. bumps & balls)

Requirement:
Interconnect path dedicated for SJ BIST

# SJ BIST Application

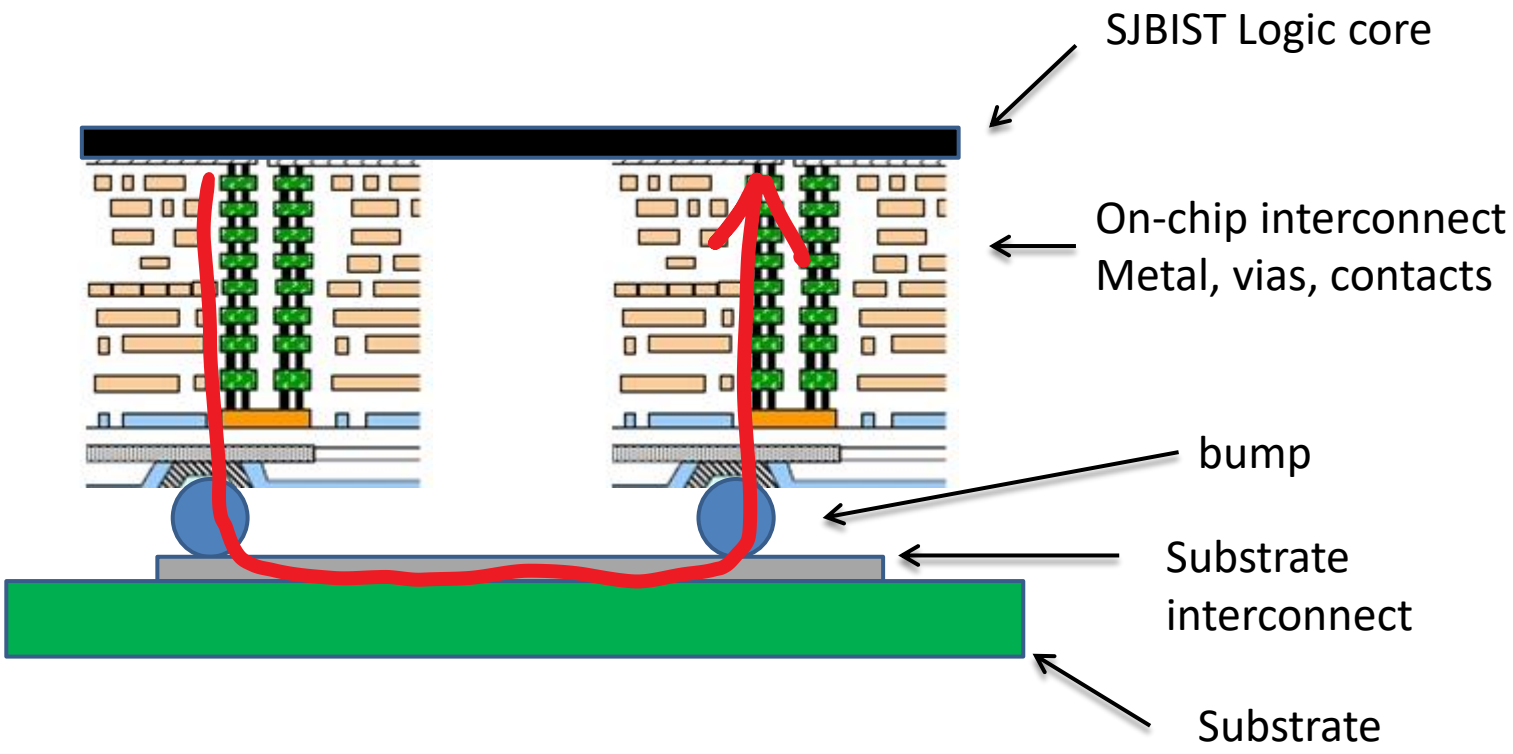
Testing On-chip Interconnect




**Need for dedicated on-chip path between SJ BIST™ Observation pins**

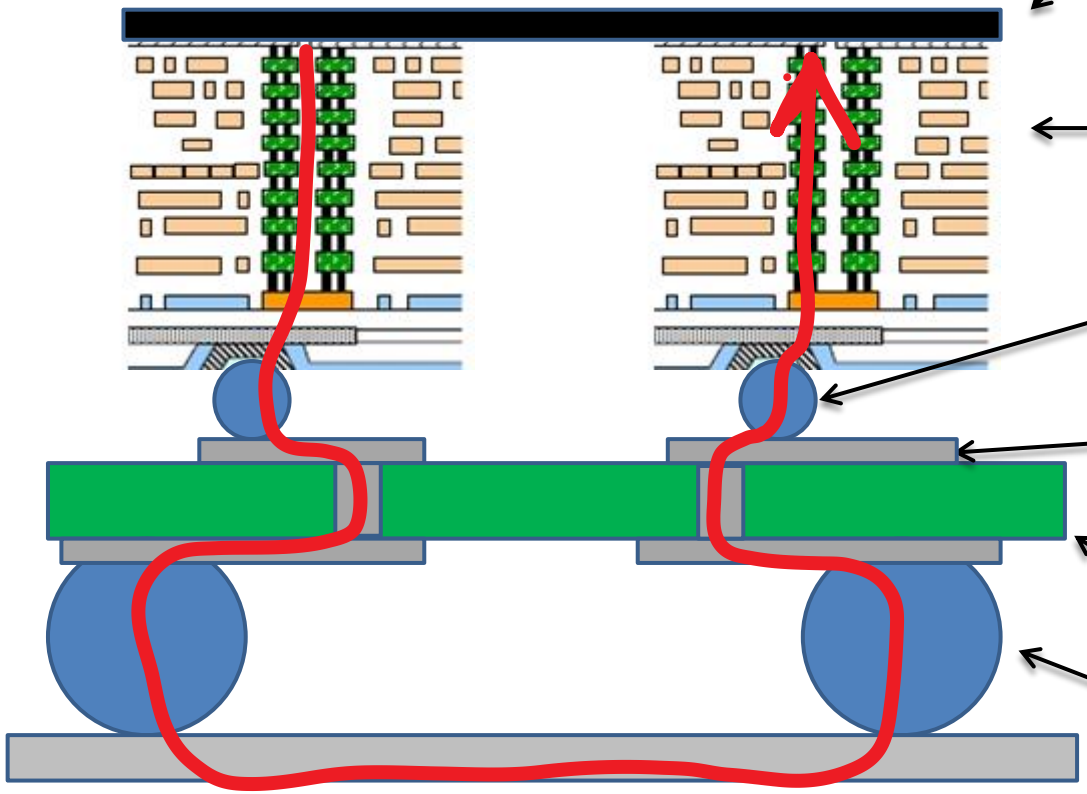
# SJ BIST Application

Testing Die to Substrate



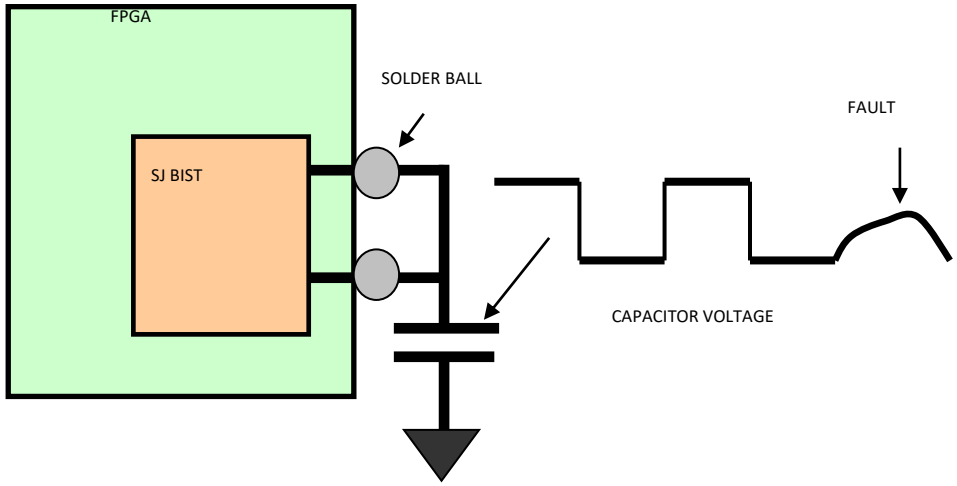
# SJ BIST Application

Testing Die to Board



# SJ BIST Simulation Results

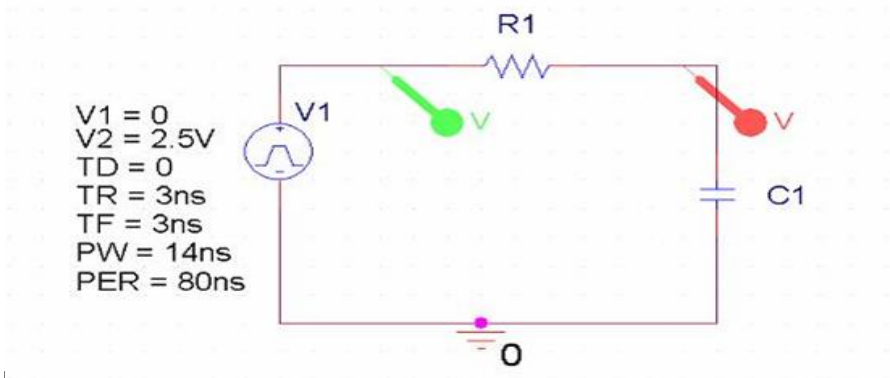
## LVTTL – Low Voltage TTL




| Output | |
|---|---|
| Low | High |
| ≤0.4V | ≥2.4V |

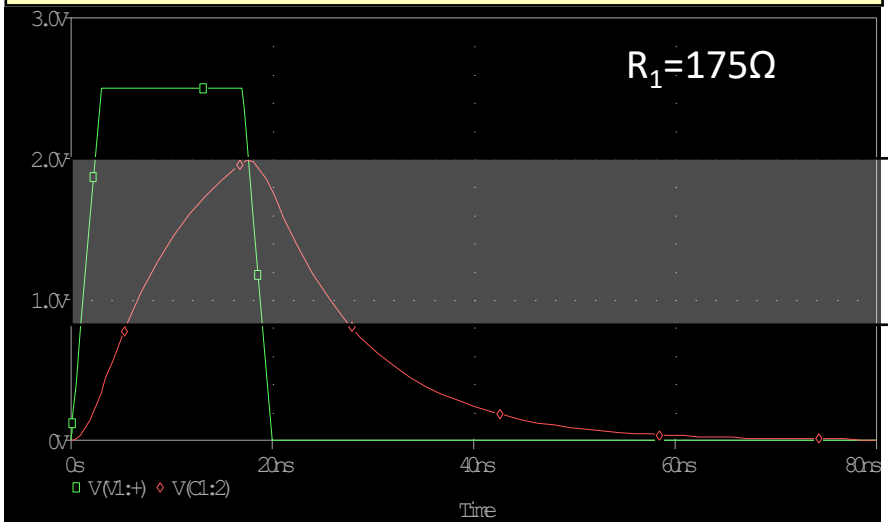
| Input | |
|---|---|
| Low | High |
| ≤0.8V | ≥2.0V |

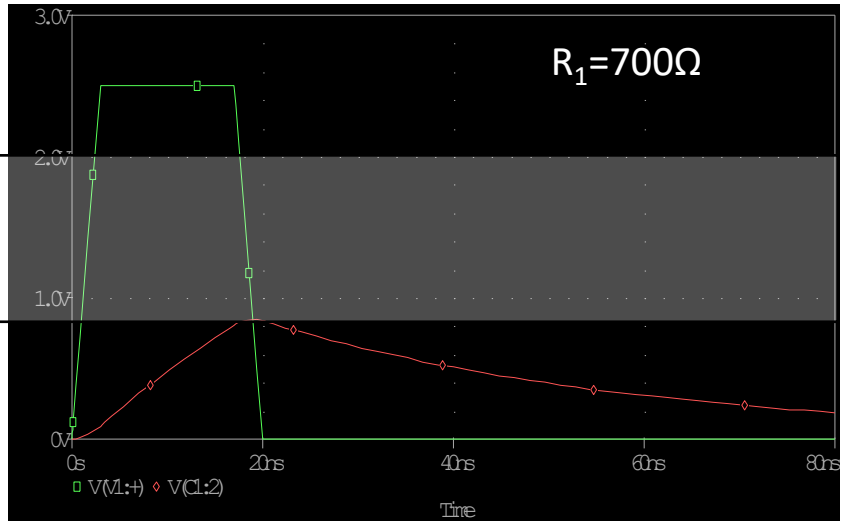
# SJ BIST Simulation Results



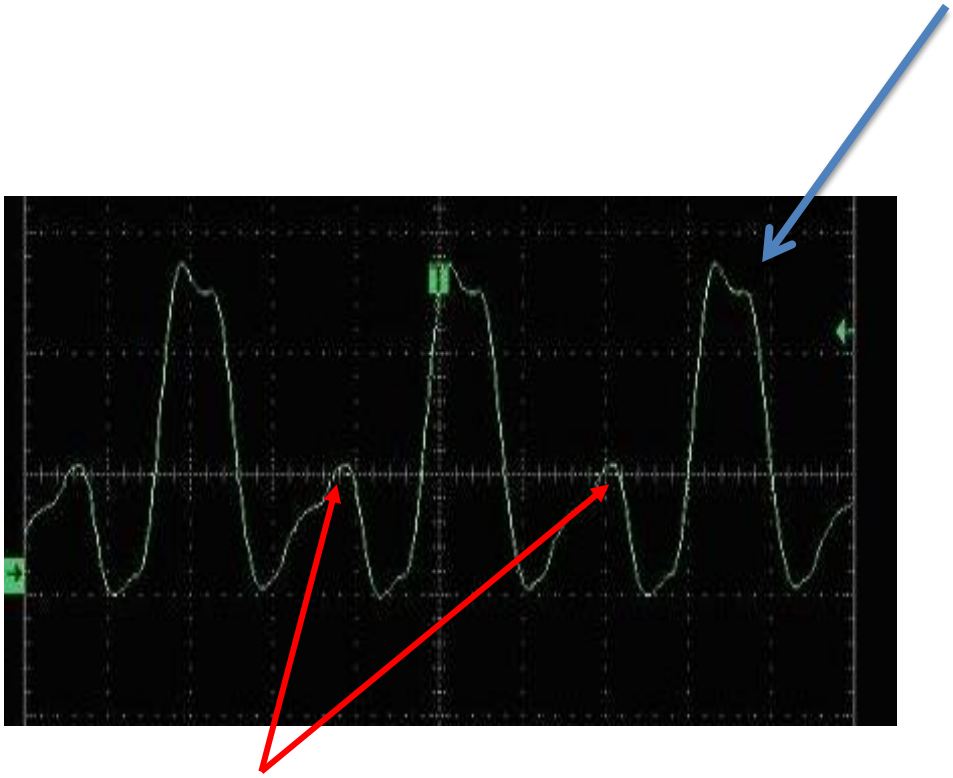

- Clock = 50 MHz
- Charge pulse t=20 ns
- $C_1$=57 pF (47 pF capacitor)+(10 pF of the I/O port and wires)
- The time constant $\tau=R_1 \cdot C_1$ and t determine the charge voltage
- In the prohibited zone (0.8 to 2.0 V) there is guaranteed detection

Capacitor charging $U_C = U_0\left(1 - e^{-\frac{t}{R1 \cdot C1}}\right)$



# SJ BIST Simulation Results



Voltage across the test capacitor

One bump is connected with a 700 Ω resistor. So the time constant $\tau = R_1 \cdot C_1$ increases and the test capacitor is charged with only 0.8 V.

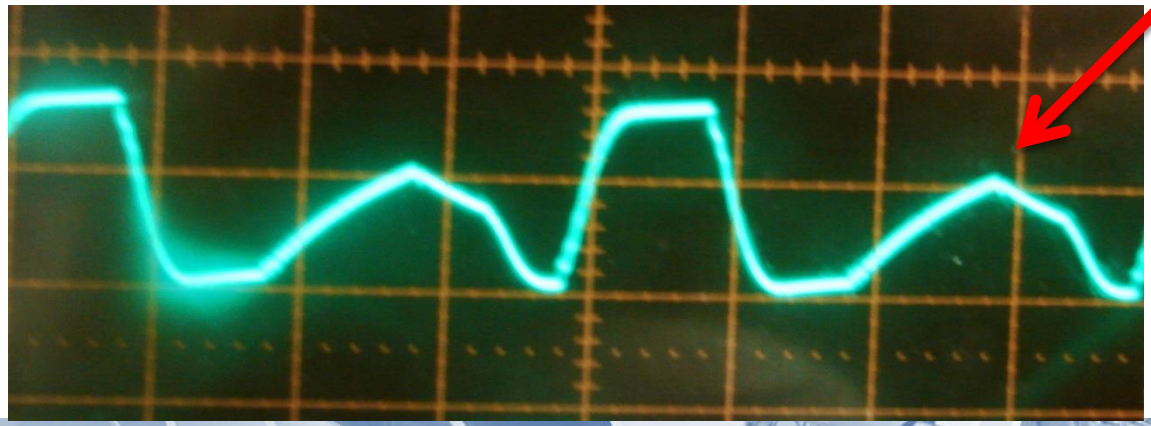
A logical ‘0‘ instead of a ‘1‘ is read, a fault is detected.

700 Ω Fault: Same as electrical model and PSPICE simulation

# SJ BIST Application Results

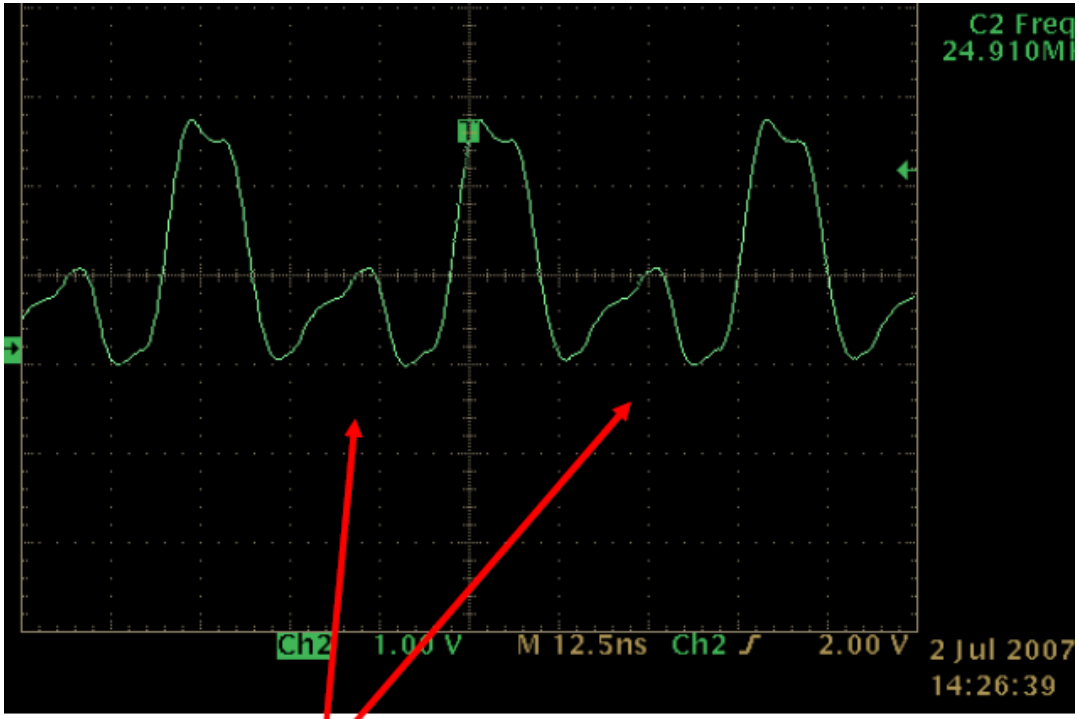
- SJ BIST specifications
  - Sensitivity: as least as low as 100 Ω
  - Resolution: guaranteed two clock periods
  - Detectable intermittency: as short as ½ of a clock period
  - 50 MHz clock
    - 40-ns guaranteed detection
    - 10-ns detection possible

100 Ω fault
1 MHz clock



# SJ BIST Application Results

- Independent test results by German automotive firm
  - Confirmed the same results as obtained by Ridgetop Group
  - No false alarms



# SJ BIST I/O

- Input (Control)
  - Clock, Enable & Reset
- Test Pins
  - 2 bidirectional I/O pins: TP0 & TP1
- Output (to host)
  - Failure Flags (fault was detected on TP0/TP1)
  - Active fault flags (fault is active on TP0/TP1 at the moment of interrogation of SJ BIST)
  - Failure counts (2 8-bit values related to number of faults detected on TP0 and TP1 respectively)

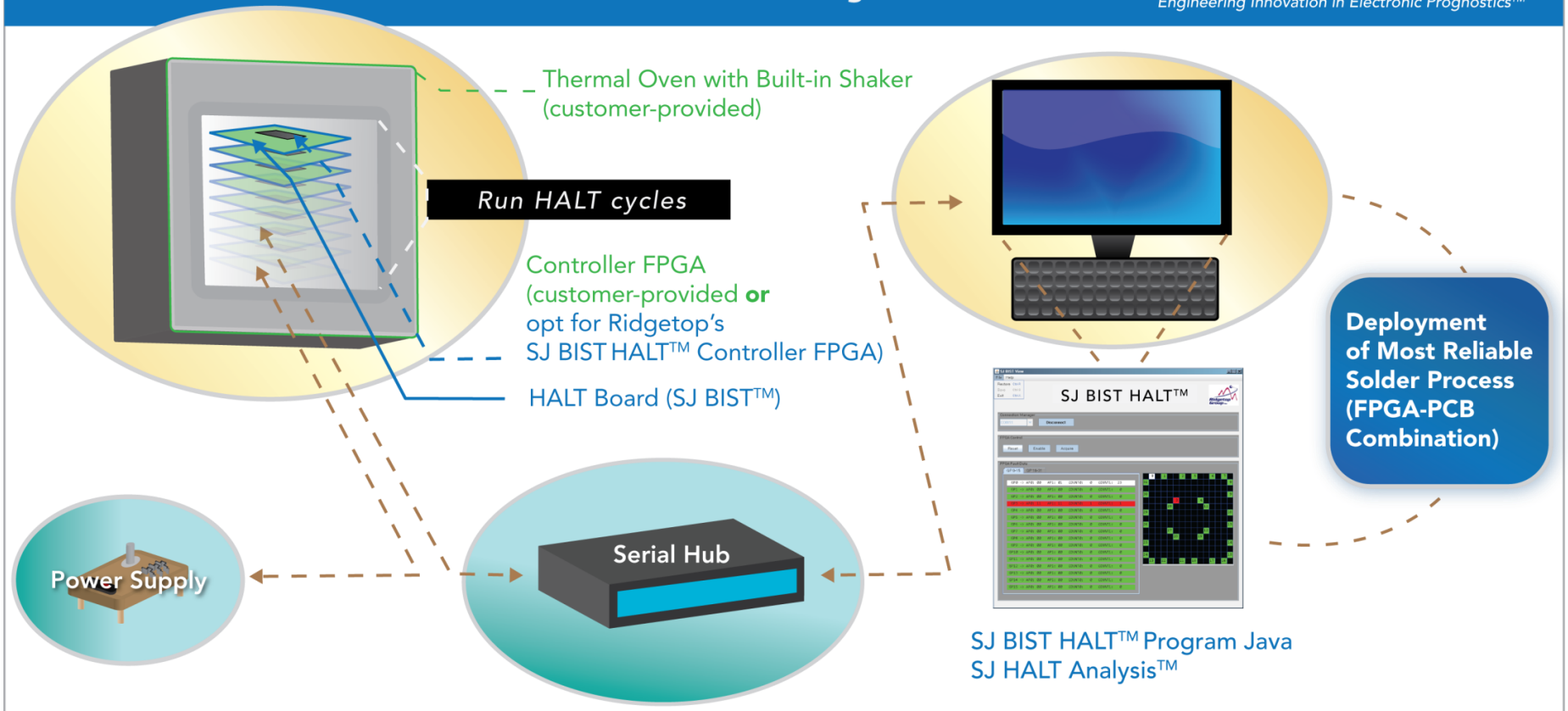
# SJ BIST Summary

- Available as:
  - Verilog/VHDL core
  - Microcontroller code
- Requires dedicated I/O + capacitor
- Runs concurrently
- Interconnect reliability verification
  - Process qualification
  - Lifetime observation

# SJ BIST HALT for Process Qualification

## Q: What can SJ BIST HALT™ do for you?

Ridgetop Group Inc
Engineering Innovation in Electronic Prognostics™




**A: Provide a cost- and time-saving search method for the most reliable solder process (FPGA-PCB combination).**

# Contact Information

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