High Density FPGA Package BIST Technique

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Abstract

Over 81% of new digital designs utilize Field Programmable Gate Arrays (FPGA's). With FPGA packages exceeding 1000 pins, with Ball Grid Array (BGA) solder bumps providing the interconnect, it is vitally important to make solid contact with the Printed Circuit Board (PCB).

Unfortunately, these solder bumps are subject to the effects of aging, which encompasses cracking of the solder ball, oxidation within the crack and eventual failure of the connection. Although the failures are metallurgically-based, the effects can be detected electrically using a verilog softcore and in-situ sensor during the power-on self testing sequences.

Ridgetop will describe its work in providing a self-contained built in self test (BIST) solution that is effective in detecting the degradation and eventual failure of the FPGA.

Introduction and growth in use of BGA packages for FPGAs

In recent years, Field Programmable Gate Arrays (FPGAs) have advanced greatly in their capability. The corresponding needs for I/O on these devices have compelled the manufacturers to utilize high-density ball grid array (BGA) packages, now with configurations exceeding 1,000 pins with very narrow solder bump pitches. According to a recent EE Times Survey, over 81% of new digital designs incorporate FPGAs[1].

BGAs fit the FPGAs into a smaller footprint, decreasing pitch spacing, by utilizing an array of solder ball connections. This allows for a higher density of I/O connections than other package types. The result is a considerably smaller finished package size.

While BGAs feature shorter electrical path lengths which reduce inductance, the critical solder bump connections are subject to aging and eventual failure from a cracking, oxidation and failure progression.   Ridgetop has developed a Built-In-Self-Test (BIST) core that can be used to detect impending problems on FPGAs, so that mitigating actions can be taken.
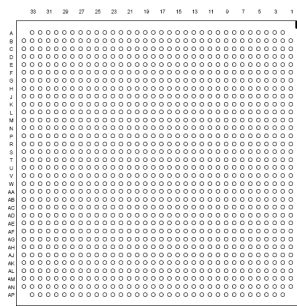
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[1] EETimes, June 5, 2006
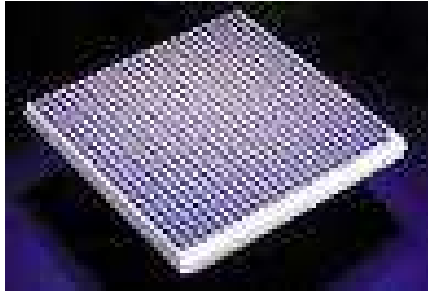
Figure 1 – Typical Ball Grid Array Package (*from Chip Scale Review*)

The top-down view of a high density package is shown in figure 2 where extremely high pitches are involved.


Figure 2 – Top-down view of the solder bump mapping. The solder bumps can be 0.6mm in diameter and placed on 1 mm center to center.

Points of Failure: BGA Solder Joints

The following is a list of some points of failure associated with FPGAs in BGA packages: (1) the junction between the FPGA package and the solder ball, (2) the junction between the solder ball and the printed wire board and (3) the wire bond lift off or break within the FPGA package.

The most typical failure point is the junction between the FPGA package and the solder ball as depicted in **Figure 3.**
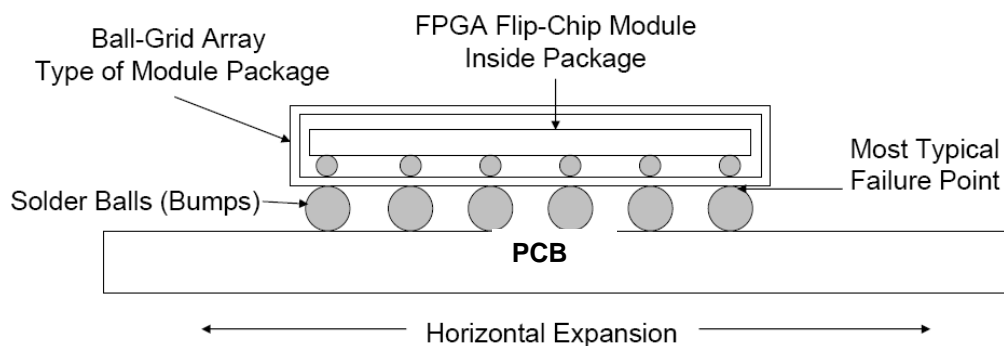

Figure 3: BGA Solder-Joint, Solder Balls and Typical Failure Point.

A typical failed joint using results from Auburn University is shown in figure 4.

Figure 4 – Solder bump cracking (*from Auburn University*)

While the high-resistance spike profile shown in **Figure** is simulated, the results have been verified by Highly Accelerated Life Test (HALT) experiments conducted at the Center for Automotive and Vehicle Electronics (CAVE) at Auburn University with whom Ridgetop maintains a research partnership.
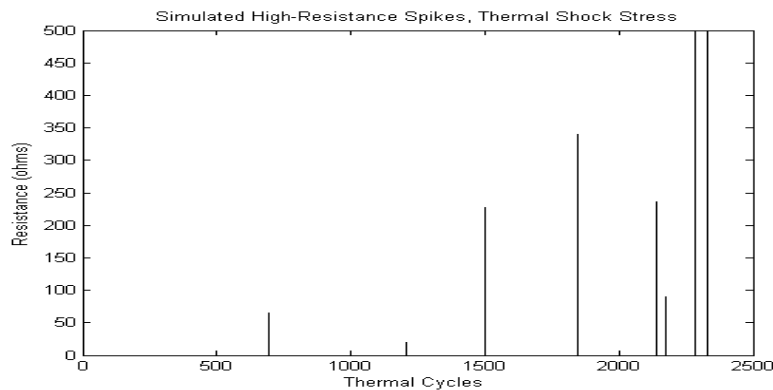
Figure 5: Solder-Joint Resistance Profile Showing Presence of High Resistance Spikes.

Definition of Failure

One industry standard for defining a BGA package failure during a test involving thermal cycles, with or without accompanying physical stresses, is given below:

1. An event is defined as the occurrence of a high-resistance spike of 300 ohms or higher for a duration period of 200 nanoseconds or longer.

2. A BGA package failure is defined as the occurrence of 10 or more events that occur within 10 percent of the time (number of thermal cycles) of the first event.

By this standard, a BGA assembly that exhibits intermittent, high-resistance spikes as shown in Figure is deemed not to have failed because (1) the first event occurred at about 700 cycles and (2) at no time during the remaining test cycle did the BGA package exhibit 10 events within 70 cycles: in fact, a total of only three events occurred: five of the relatively high-resistance spikes are, by definition, not events. The Ridgetop solder-joint fault detectors are able to detect high-resistance spikes of 10s of ohms.

The occurrence of a single high-resistance spike is indicative of solder-joint damage, and the package has reduced reliability. The use of that component might not be prudent in a mission-critical situation. Because solder-joint fatigue damage is accumulative, the occurrence of just a couple of high resistance spikes, and perhaps just one, is indicative that the PCB assembly is likely to exhibit intermittent failures, especially when subjected to stresses associated with vibrations such as with automotive or vehicle applications.

Ridgetop's BIST Approach

Ridgetop's test approach was to provide a hardware/software BIST solution. The first step is to use otherwise unassigned pins on the FPGA for use in the test structure. This pin becomes the monitor pin and represents a precursor to a more serious impending failure of the FPGA.

Verilog softcore was written that can be incorporated into the built-in test backbone of the device (to be used possibly on power-up), and a small capacitor that accompanies each of the unused test points on the package, as shown in figure 6. The softcore provides for the generation of the test sequence shown in figure 6.
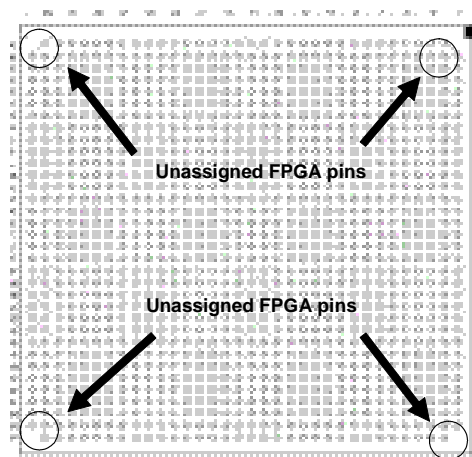

Figure 6 – The test points are usually unassigned pins at the ends of the package, where the maximum bending point occurs.
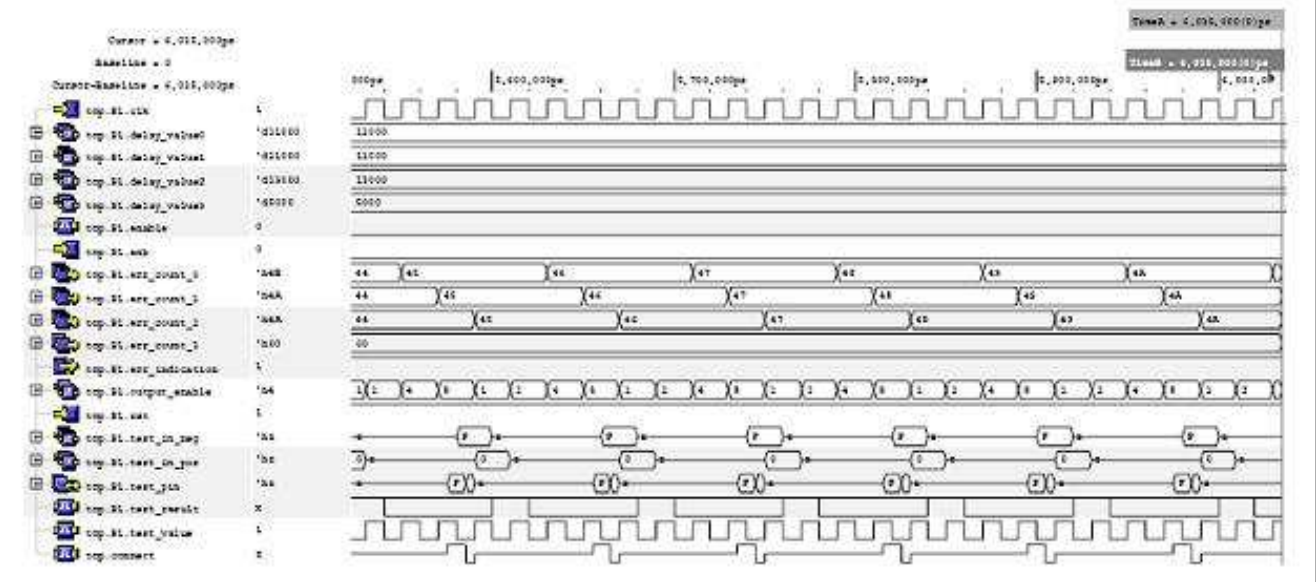

Figure 7 – Test code generation example

The test code generates a pulse train that is used to detect the 1's and 0's. If there is a high resistance path through the solder ball, indicating a high resistance or open, then the reflected pulse amplitude will be low as shown in figure 8. This is a detected fault at the outer sacrificial pin. It is inferred that the inner pins (where there are programmed cells critical to the FPGA operation) will fail later. This approach provides an early-warning electronic prognostic of the impending failure of the entire package.
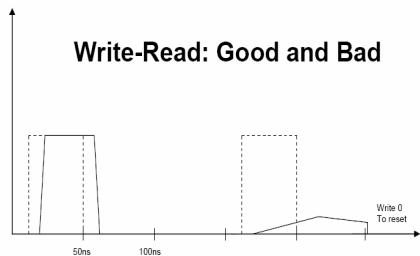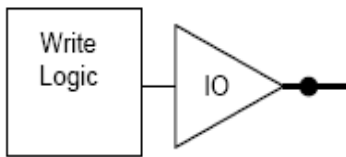
Figure 8 – Write/Read Pulse analysis. A low response indicates a high-resistance path, which is indicative of a faulty solder ball.

Actual measurement results taken are shown in figure 9.
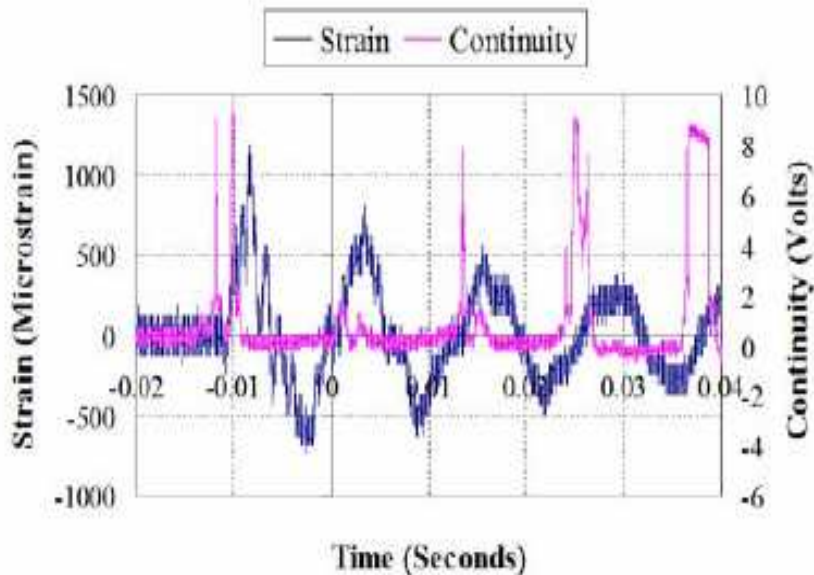
Figure 9 – Measurement results showing applied strain and intermittent continuity through the solder ball.

Electronic Prognostics and the Reliability Bathtub Curve

Failure probability for a device typically follows a bathtub curve (**Figure**), with three distinct regions:

- Infant Mortality (Burn-In) Region. High probability of failure, related to manufacturing defects.
- Useful Life Period. Minimum, almost constant failure rate caused mostly by temperature, vibration and voltage stresses.
- Wearout (End-of-Life) Region. Due to wear out or fatigue mechanisms, probability of failure increases.
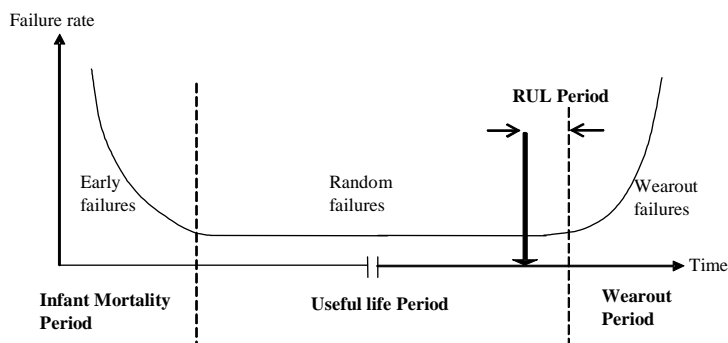
Figure 10: Bathtub Curve Showing Failure Rate with Time, along with Remaining Useful Life (RUL) period

The failure of a edge pin on the FPGA represents a precursor event to an impending failure of the FPGA. The fault to failure progression depends on the package type, the type of solder used, and number of pins used. Ridgetop is continuing to gather statistics that will provide better estimates of the RUL period for a series of intermittent spikes occurring on the FPGA packages.

Summary

Ridgetop has developed an effective means of testing the integrity of Ball Grid Array (BGA) packages as used in FPGAs and embodied this technology into a product called InstaBIST™ BGA. This IP consists of a Verilog Core and Documentation to enable on-going testing of the BGA packages that are deployed in critical applications.

Acknowledgements

Ridgetop would like to acknowledge the assistance of the NAVAIR/JSF Program Office, Raytheon Corporation, and Center for Automotive and Vehicle Electronics at Auburn University for their support of this work.

References

[1] D. Love and D. Towne, BGA Reliability Characterization Project Temperature Cycling Tests, Sun Microsystems, Palo Alto, California, USA, January, 1999

[2] PEM Qualification Requirements for Radiation Hardened non-hermetic products qualifiable for space flight applications

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