A Low-Power Sensor Design, SJ Monitor, for Monitoring 24x7 the Health of BGA Solder Joints

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Abstract—As FPGA density and overall usage increases, there is a corresponding and growing need to monitor these solder-joint networks. Prior to the introduction of a first sensor, SJ BIST™ (SJ Built-in-Self-Test™), there were no known methods for detecting faults in the solder-joint networks of fully-programmed, operational Field Programmable Gate Arrays (FPGAs). Because SJ BIST™ requires over 100 mW at 3.3 V to test 8 FPGA pins, we introduce SJ Monitor™, a lower-power design (less than 5.0 mW) to provide 24x7 health monitoring of selected I/O pins; the complementary form SJ Monitor™, can be used to monitor the pins of un-powered FPGAs. SJ Monitor is able to detect all solder-joint network faults that last at least as long as 15 nsec and which are at least as low as 100 Ω with no false alarms. This capability allows for detection of faults before they begin to exhibit intermittent failures, which in turn facilitates condition-based maintenance to reduce failures during critical missions[1][2].

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1. INTRODUCTION

FPGAs are widely used as controllers in aerospace applications, and modern FPGAs, such as a XILINX® FG1156, have over a thousand pins, each of which is part of a solder-joint network and each of which is prone to becoming damaged and causing intermittent faults. As FPGA package density increases and as the use of FPGAs increases, there is a corresponding increase in need to monitor those solder-joint networks: Being able to detect solder-joint faults increases both fault coverage and health management capabilities and provides support for comprehensive condition-based and reliability-centered maintenance. Prior to the introduction of the first sensor, SJ BIST™ (SJ Built-in-Self-Test™), there were no known methods available for detecting faults in the solder-joint networks belonging to fully-programmed, operational Field Programmable Gate Arrays (FPGAs) especially FPGAs in Ball Grid Array (BGA) packages such as a XILINX® FG1156 [1-6].

In this paper, we introduce a low-power sensor design, SJ Monitor™, which uses innovative circuit design on an Integrated Circuit (IC) chip in-situ on an FPGA's board to provide a method to monitor 8 I/O pins 24x7 for solder-joint faults and which uses less than 5.0 mW. SJ Monitor is able to detect all solder joint faults of at least 100 Ω (sensitivity) that last at least as long as 15 ns (resolution)—with no false alarms. The complementary form of SJ Monitor™ can be used to monitor the pins of powered-off FPGAs.

Mechanics of Failure

Solder-joint fatigue damage caused by thermo-mechanical and shock stresses is cumulative and manifests as voids and cracks, which propagate in number and size. Eventually, the solder ball (or bump) of the joint fractures [7-10] and FGPA operational failures occur.

An illustration of a damaged solder bump on the verge of fracturing is shown in Figure 1. Figure 2 and Figure 3 depict a cracked solder ball of a BGA package attached to an electronic printed circuit board (PCB); Figure 4 depicts a fractured solder ball, which is what happens to a crack as an end result of accumulated fatigue damage. A fracture is the complete separation of a solder ball that can result in a break in the electrical connection between the BGA and the

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[1] 1-4244-1488-1/08/$25.00 ©2008 IEEE.
[2] IEEEAC paper #1149, Version 5, Updated 2007:10:23.

electronic board.

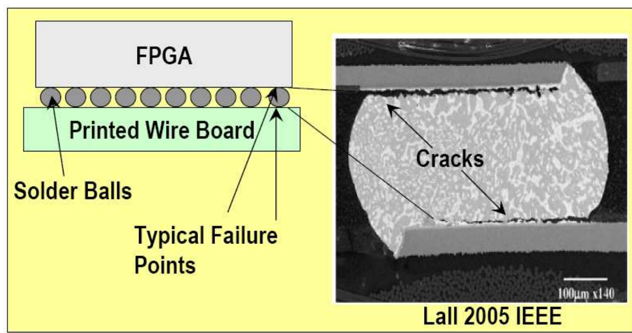

Figure 1: Cracked Solder Ball (Bump), 15mm BGA [8].

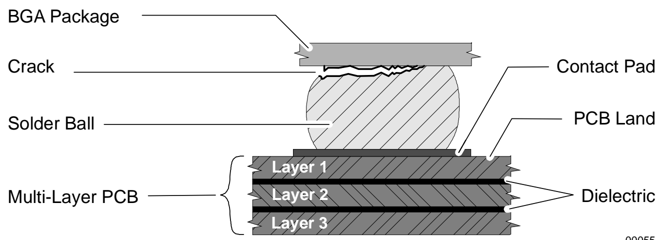

Figure 2: Crack at BLM-Solder Ball Junction.

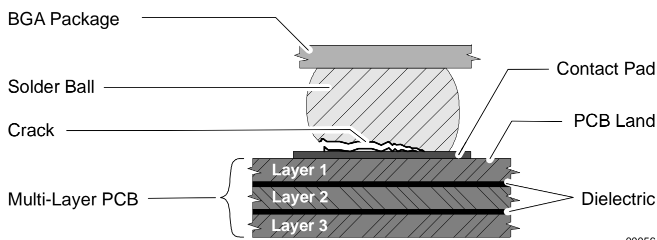

Figure 3: Crack at Solder Ball-PCB Junction.

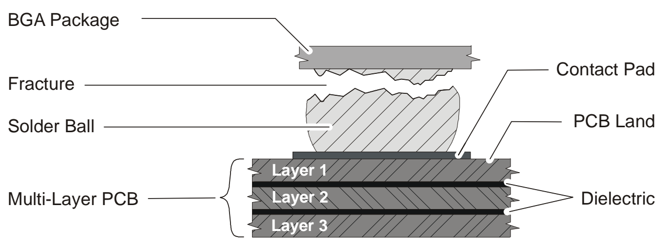

Figure 4: Fractured Solder Ball.

Intermittent Behavior of Fractured Solder Bumps

Over time, contamination and/or oxidation films form on the fractured surfaces and a failure progression occurs: from degraded joints to intermittent opens of short duration (nanoseconds or less) to longer durations (microseconds) to very long durations (milliseconds or longer). The latter case, with intermittent faults lasting milliseconds or longer, are very likely to cause faults in the correct FPGA operation. Test results confirm this physics of failure behavior. As seen in Figure 5, during periods of high stress, fractured bumps tend to momentarily open and cause hard-to-diagnose, intermittent faults of high resistance of 100s of Ohms [10-12]. Such faults typically last for periods of hundreds of nanoseconds, or less, to more than 1 µs [7, 11, 13-16]. The intermittent faults are caused by the opening and closing of the fractured faces of the solder balls (see Figure 6).

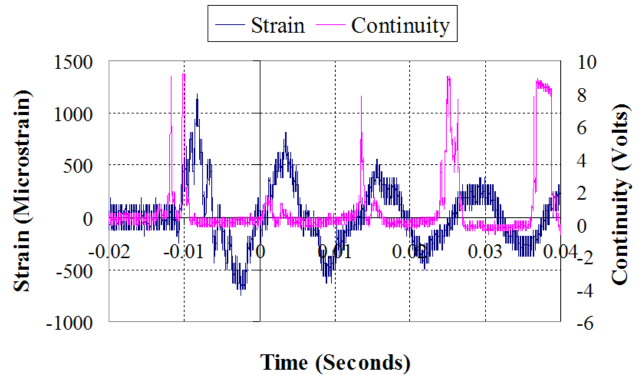

Figure 5: Shock-actuated Failure: Transient Strain (Blue) and Intermittent Opens (Mauve) (From Lall).

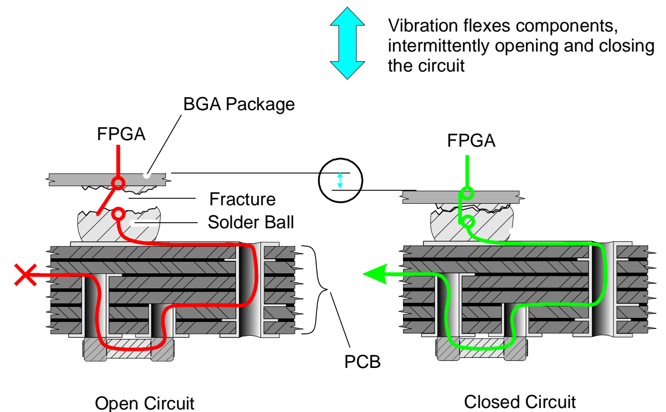

Figure 6: Intermittent Open and Closed Connection.

These intermittent faults increase in frequency as evidenced by a practice of logging BGA package failures only after multiple events occur of high-resistance: an initial event followed by some number (for example, 2 to 10) of additional events within a specified period of time, such as ten percent of the number of cycles of the initial event [14-16]. Even then, an intermittent fault in a solder-joint network might not result in an operational fault. For example, the fault might be in a redundant ground or power connection; or it might occur during a period when the network is not being written; or it might be too short in duration to cause a signal error. In Figure 5, the duration of the fault in the 5th cycle of stress is over 3 milliseconds.

Damage accumulates and eventually there is a catastrophic failure of the FPGA, such as might happen when a solder ball becomes displaced as depicted in Figure 7. Figure 8 represents Highly Accelerated Life Test (HALT) results performed on XILINX FG1156 Daisy Chain packages in

which 30 out of 32 tested packages failed in a test period consisting of 3108 HALT cycles. Each temperature cycle of the HALT was a thermal transition from -55 °C to 125 °C in 30 minutes: 3-minute ramps and 12-minute dwells. What is not immediately apparent is that each of the logged FPGA failures (diamond symbols) represents at least 30 events of high resistance: a FAIL was defined as being at least 2 OPENS within the same temperature cycle. A single OPEN in any temperature cycle was not counted as a FAIL event; and the package was deemed as failed only after 15 FAILS [15] had been logged.

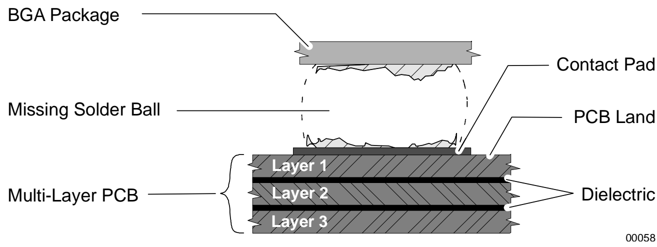

Figure 7: Displaced (Missing) Solder Ball.

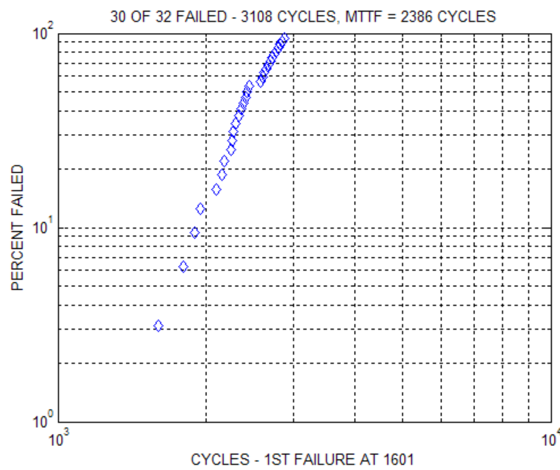

Figure 8: XILINX FPGA HALT Test Results [15].

State of the Art

The use of leading indicators of failure for prognostic indication of impending failure of electronics has been previously demonstrated [17-20]. One important reason for using an in-situ solder-joint fault sensor is that stress magnitudes are hard to derive, much less keep track of [21]; another reason is that even though a particular damaged solder-joint might not result in immediate FPGA operational faults, the fault indicates the FPGA is likely to have, or will soon have, other damaged I/O ports—in short, the FPGA is no longer reliable.

FPGAs are not amenable to the measurement techniques typically used in manufacturing reliability tests such as Highly Accelerated Life Tests (HALTs) [10]. This is because, for example, a 4-point probe measurement requires devices to be powered-off; and because FPGA I/O ports are digital, rather than analog, circuits (see Figure 9).

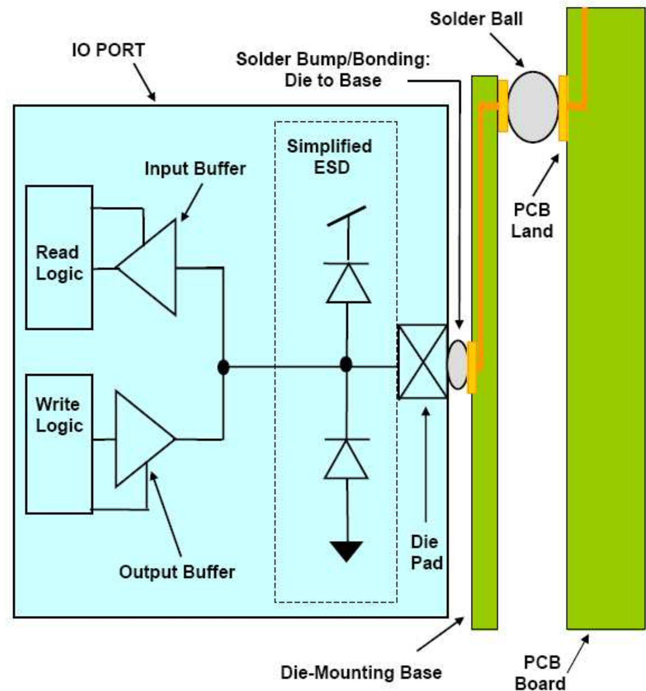

Figure 9: FPGA Diagram, I/O Buffer [22].

Modern BGA FPGAs have more than a thousand pins and very small pitch and ball sizes, for example, the left side of Figure 10 shows the position of the XILINX FG1156 FPGA die with respect to the FPGA mount, and the right side shows the bottom of the package—a footprint of 35x35 mm^2, and a 34x34 array of solder balls. The dense array of fine-pitch and ultra fine-pitch BGA packages with very small pitch and solder ball tends to make physical-, optical-, X-ray- and sonic-based inspection techniques impractical for detecting the onset of damage.

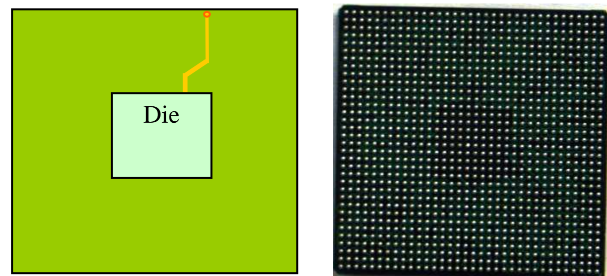

Figure 10: FG1156: Size is 35x35 mm^2; Pitch: 1.0 mm. Ball: 0.6 mm [23].

One of the Ridgetop test boards was physically ground to create the cut view shown in Figure 11. The cut view shows the FPGA die is connected by either flip-chip collapsed connections or by bonding to a die-mounting base. Wire interconnects connect the die to ball limiting metallurgy

(BLM), to which solder balls are attached. The FPGA package is then placed over connection lands on the printed circuit board (PCB) and soldered. Note the presence of voids in the two solder balls on the right-hand side of Figure 11: such voids lead to early onset of solder ball failure.

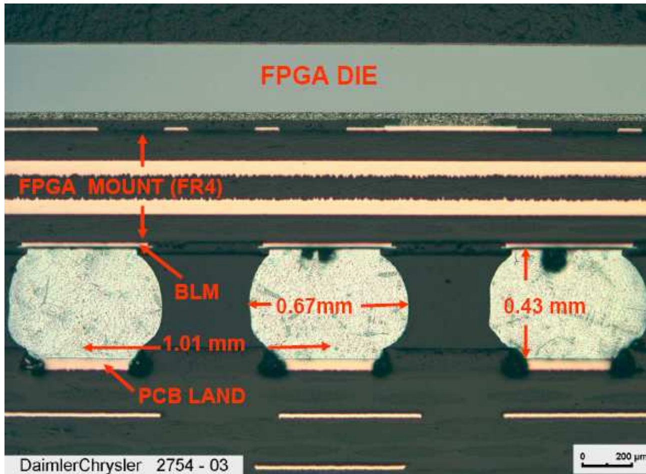

Figure 11: View Showing FPGA Die to PCB Connection.

2. SJ MONITOR

During the design and development of SJ BIST, Raytheon Missile Systems, Tucson, Arizona, asked if Ridgetop would provide a solder-joint fault solution that met the following requirements: (1) battery powered and (2) used to monitor FPGAs that were in a powered-off state. Accordingly, Ridgetop designed and developed SJ Monitor to meet those requirements.

Analog Block Diagram

SJ Monitor, as shown in the block diagram in Figure 12, is designed and is being developed as an Integrated Circuit (IC) chip, which is mounted adjacent and connected to the FPGA on the board. SJ Monitor is a low-power, continuous monitoring sensor.

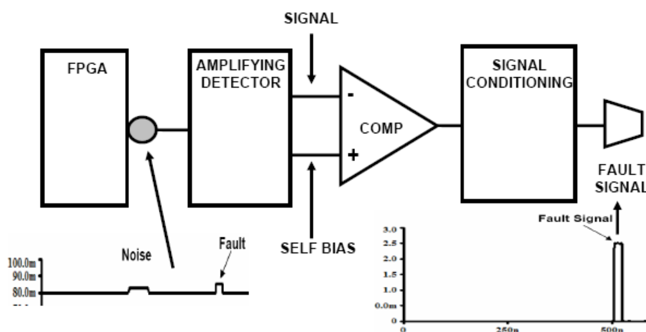

Figure 12: SJ Monitor, Analog Block Diagram.

A solder-joint fault of at least 100 Ω is detected and amplified by an amplifying detector, which also produces a self-biasing reference voltage. The circuit design is such that SJ Monitor (1) rejects all noise of 3.0 mV or less; (2) accepts all fault signals of 5.0 mV or higher; and (3) is insensitive to the exact steady-state DC voltage on an FPGA pin. The amplified analog signal from a high-gain comparator is conditioned to produce a digital pulse whenever a fault is detected. Each digital pulse is processed for Prognostic Health Management (PHM) purposes: counts, flags and health level.

SJ Monitor is fully designed and simulated at 3.3 V for a TSMC® 0.25-µm process; and at 1.2 V and 2.5 V supply voltages for the IBM® 130-nm 8RF bulk CMOS process node. At 1.2 V, SJ Monitor uses less than 5.0 mW of power, which means SJ Monitor can be used in a battery-powered, 24x7 monitoring application. There is flexibility on the number of test cells included on a single IC chip. Board wiring constraints might require 4 cells on each IC chip; in turn, this requirement might then require the placing of two SJ Monitor chips on the board.

A complementary version of SJ Monitor using negative 1.2 V power was also designed and simulated using a circuit design simulator. The complementary version provides a monitoring capability for FPGAs that are powered off. The simulation results for the complementary version are so similar to those shown in Figure 12 through Figure 16, separate figures are not provided.

Pull-down Level of FPGA I/O Ports

Measurements and evaluations of various FPGAs from more than one manufacturer indicate that for I/O ports pulled low and sourced with external currents of less than 0.5 mA, the noise on an output I/O port is less than 1.0 mV. This allowed us to design SJ Monitor to source less than 200 µA to each monitored I/O pin of an FPGA.

SJ Monitor is insensitive to the exact level of the pull-down voltage on an I/O port, and this was verified by simulations of pull-down levels from 0 to over 300 mV. The simulations included noise perturbations of 2.0 to 3.0 mV, which is about 3 times larger than the maximum level of measured noise: none of the noise perturbations caused a false alarm and all signal perturbations of 5.0 mV or larger were detected and reported as faults. The design is easily changed to produce larger sourcing currents to overcome a greater-than-expected noise margin.

Simulation Results: Noise Rejection and Fault Detection

Referring to Figure 13, (A) shows an I/O pin with a pull-down voltage level of 10 mV and (B) shows an I/O pin with a pull-down voltage level of 100 mV. Superimposed on each of the pull-down voltage levels are 3.0 mV noise pulses and 9.5 mV fault perturbations caused by injecting a 100 Ω fault into the solder-joint network. These two inputs both result in the output shown in Figure 14.

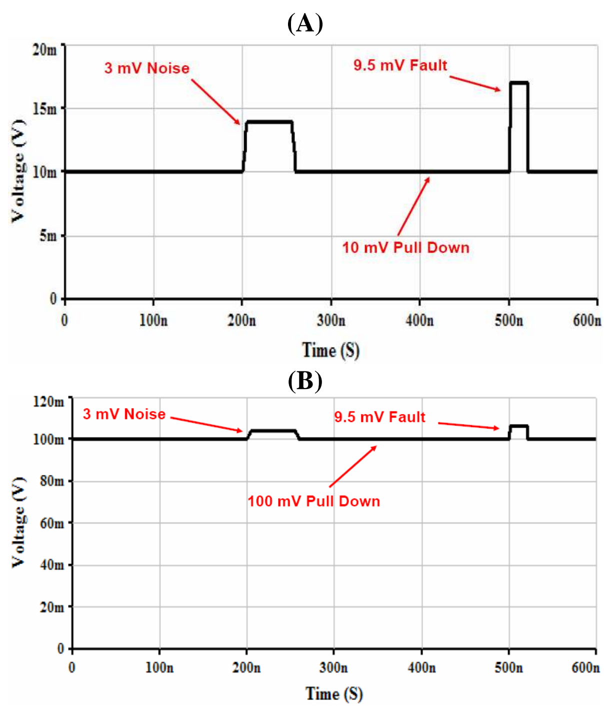

Figure 13: FPGA I/O Pin Voltages: (A) Pull-down is 10 mV and (B) Pull-down is 100 mV; Noise is 3.0 mV, Fault Perturbation is 9.5 mV.

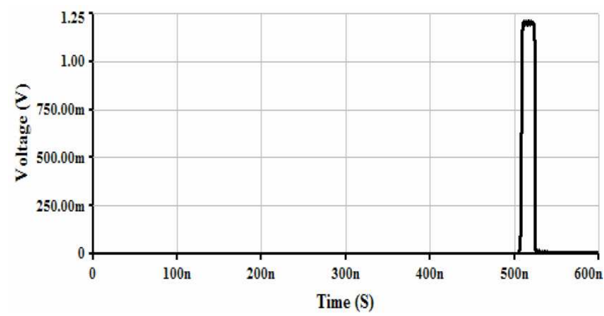

Figure 14: SJ Monitor Fault Signal Response to Figure 13 A and B.

SJ Monitor uses self-biasing and signal conditioning to ignore the pull-down voltage level, to suppress noise and to amplify the fault perturbation to produce a digital fault signal.

Simulations were performed using variations in circuit parameters: (1) 10 to 20 percent variation in transistor widths and lengths were used; (2) three different power supply voltage levels were used – 1.08 V, 1.20 V and 1.32 V; (3) three different temperatures were used – -25°C, 27°C and 100°C; and (4) the complementary version of SJ Monitor was simulated using negative power voltages of -1.08V, -1.20 V and -1.32 V. For all variations, SJ Monitor produced correct results: all faults detected and no false alarms.

SJ Monitor Sensitivity and Resolution

The value of the minimum detectable fault resistance is primarily dependent on the duration of the fault and the operating temperature as shown in Figure 15. The results indicate that SJ Monitor is able to detect a fault resistance of at least 100 Ω when the fault duration is at least 20 ns.

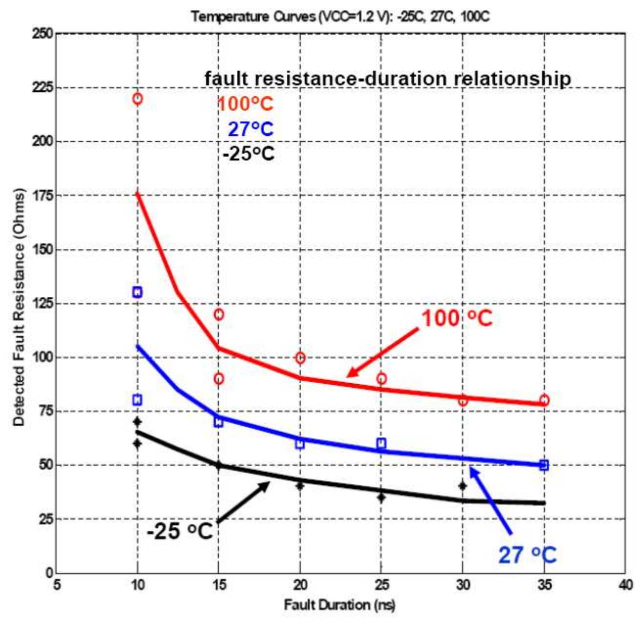

Figure 15: Temperature, Fault Resistance and Fault Duration Curves.

SJ Monitor Power

Test simulations showed SJ Monitor has a power requirement of between 0.9 mW and 2.4 mW (Figure 16) to monitor 8 I/O pins, depending on temperature and voltage. This low power requirement makes SJ Monitor suitable for continuous monitoring and for short test applications.

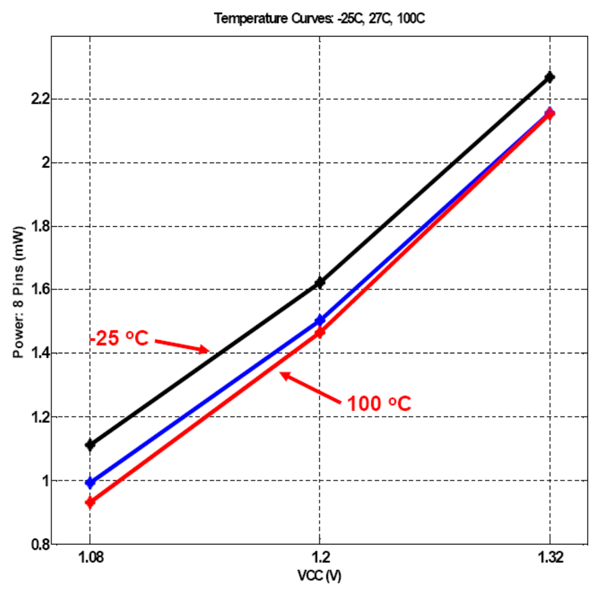

Figure 16: Power, Temperature and Supply Voltage.

SJ Monitor Signals

SJ Monitor has the following signals for each monitored pin: (1) currently active fault; (2) at least one fault detected; and (3) 1:255 count of the number of faults detected. Common control input control signals are (1) enable monitoring and (2) reset counts and flags.

3. INTERMITTENCY MITIGATION

SJ Monitor is a very useful sensor for mitigating intermittencies. Early detection of failure of an unused I/O pin allows the electronic board to be replaced before subsequent fatigue damage causes an application I/O pin to fail, and therefore intermittent operational anomalies are avoided.

Intermittent Behavior of Fractured Solder Joints

As previously seen in Figure 5, fractured solder joints tend to maintain electrical contact until periods of increasing stress occur: a hard open longer than a millisecond did not occur until the fifth shock wave. SJ Monitor would have recorded at least eight instances of faults: two in each of the first three waves and one each in the fourth and fifth waves

Intermittent Confirmation and Prognostic Warning

Detection of intermittent faults can be used to confirm that the electronic board with that FPGA is a likely candidate for replacement to address reported operational anomalies. In the absence of any reported operational anomalies, detected faults can be used as a prognostic warning that the board is likely to experience future operational anomalies.

4. PIN SELECTION

A deployed FPGA should not use the 8 I/O ports nearest the 4 corners of the FPGA package (the pink-shaded pins in Figure 17; instead those ports should be pulled low and should be attached via wiring to a monitoring pin on the chip package for SJ Monitor—we might change the recommendation to "near each corner of FPGA die shadow." Research, such as the strain diagram in Figure 18 [24], indicates the solder balls nearest the corner of the package or the FPGA die are most likely to fail first. In Figure 18, the areas of high strain are yellow-red in color, and the areas of low strain are blue in color.

High stress/strain caused by physical mounting coupled with thermal-mechanical stresses and strain are the most likely cause of the observed failure distribution of solder balls in BGA packages. Further evidence of the validity of these observations is the reserving of the four I/O pins at each corner for ground and all of the pins under the die for power and ground (the orange-shaded pins) in Figure 17.

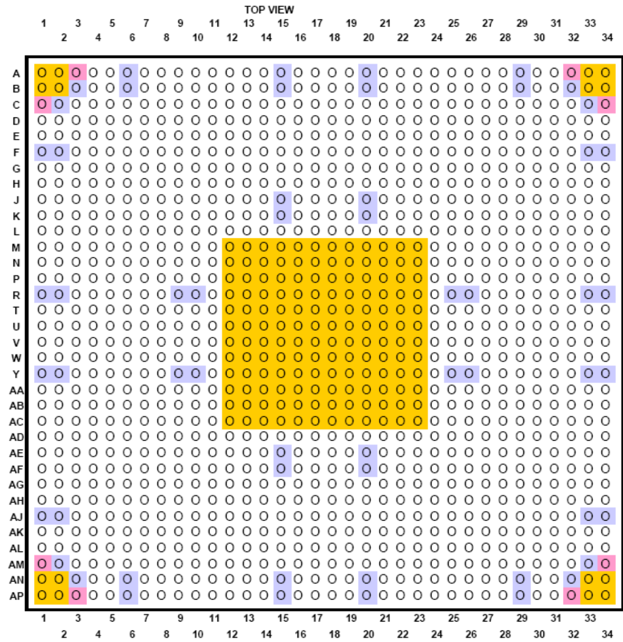

Figure 17: FG1156 I/O Pin Footprint [22].

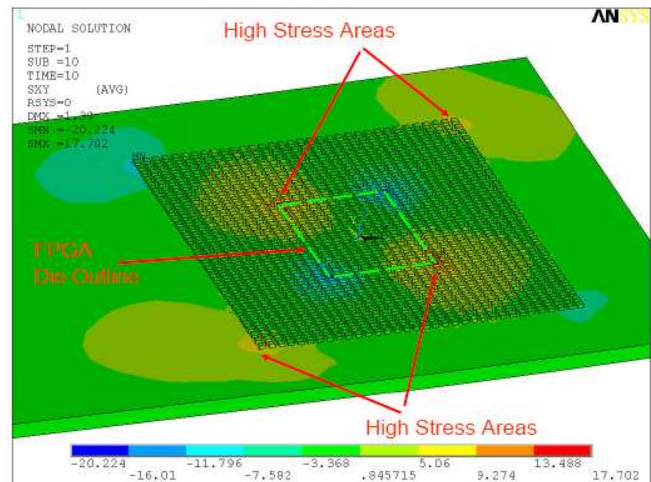

Figure 18: FG1156 Strain Diagram [24].

5. PRESENT ACTIVITIES

The detailed design and simulation of the analog circuits used in SJ Monitor were accomplished using internal research and development (IR&D) funding. We are using the same digital circuit building blocks in multiple projects to leverage our work. The tape out for the test circuitry blocks occurred late September of 2007.

6. FUTURE ACTIVITIES

The steps necessary to reach Technology Readiness Level (TRL) 6 are the following: (1) complete the IC layout and masks for both the analog and digital circuits; (2) fabricate and package SJ Monitor; (3) perform extended evaluation tests, make any required and desired circuit changes and fabricate and package in a final-form factor; (4) perform all tests required for a Silicon Validation Report (SVR); and (5) write the SVR and an initial data sheet specification.

7. SUMMARY AND CONCLUSION

In this paper we introduced a new solder-joint fault sensor, SJ Monitor. A brief overview of the mechanics-of-failure was included: the primary contributor to fatigue damage is thermo-mechanical stresses related to coefficient of thermal expansion (CTE) mismatches, shock and vibration, and power on-off sequencing. Solder-joint fatigue damage can result in fractures that cause intermittent instances of high-resistance spikes that are hard-to-diagnose. In reliability testing, OPENS (faults) are often characterized by spikes of 200 Ω or more lasting for 200 ns to 1 µs or longer.

Prior to SJ BIST, also presented in this conference, and SJ Monitor, there were no known methods for detecting high-resistance faults in solder-joint networks belonging to the I/O ports of operational, fully-programmed FPGAs. SJ Monitor is designed to be a low-power monitor for 24x7 applications, it can be battery-powered and the complementary version of SJ Monitor monitors the pins of powered-off FPGAs.

SJ Monitor to test or monitor selected I/O pins is useful because stress magnitudes are hard to derive, which leads to inaccurate life expectancy predictions; and even though a particular damaged solder-joint port might not result in immediate FPGA operational failure, the damage indicates the FPGA is no longer reliable.

8. ACKNOWLEDGEMENT

The work presented in this paper was partially funded by Small Business Innovation Research contract awards from the Department of Defense, Naval Air, Joint Strike Fighter program: Contract No. N68335-06-C-0356 P00002. Final patent applications have been filed: one for SJ Monitor technology; one for a related SJ BIST technology. U.S. Patent 7,196,294, Mar. 27, 2007, has been issued for a third related technology.

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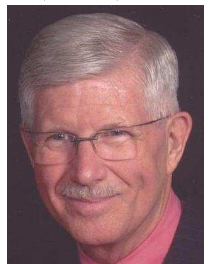

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