Vendor: Ridgetop Group, Inc.

Office Address: 3580 West Ina Road, Tucson, Arizona 85741
Phone: 520-742-3300; Fax: 520-544-3180

Technical Contact: Esko Mikkola, Ph.D., Project Manager
Phone: 520-742-3300
Fax: 520-544-3180
Esko.Mikkola@RidgetopGroup.com

ProChek™, A COMPREHENSIVE FABRICATION PROCESS MISMATCH AND RELIABILITY CHARACTERIZATION TOOL

1 Introduction

This paper provides information on ProChek™, the comprehensive process mismatch and reliability characterization tool for advanced transistor technologies. Ridgetop Group Inc. has extensive experience in the design of mixed-signal components and reliability test structure designs for advanced technology microelectronics applications. This paper describes Ridgetop's reliability evaluation capabilities and demonstrates how these capabilities uniquely support IC designers' needs.

1.1 Structure of This Paper

Section **2** is a brief statement of the reliability challenges of advanced CMOS technologies.

Section **3** discusses Ridgetop's ProChek, the innovative reliability evaluation tool for advanced processing technologies.

Section **4** introduces Ridgetop's other products that are related to ProChek.

Section **5** summarizes the discussions.

Section **6** provides company info and contacts.

2 Advanced CMOS Reliability Challenges

Increasing circuit performance demands access to advanced semiconductor fabrication processes, yet reliability and schedule requirements create obstacles to using these increasingly complex technologies. Successful technology insertion requires knowledge of failure mechanisms, design limitations, and screening flow.

Modern nanotechnology CMOS circuits have numerous reliability concerns that have to be accounted for during design and verification cycles. The circuits age during the operational life due to effects such as negative and positive bias temperature instabilities (NBTI, PBTI), time-dependent dielectric breakdown (TDDB), stress-induced leakage current (SILC), hot carrier (HC) damage, electromigration (EM), and stress migration (SM). The varying temperature extremes experienced by circuitry during operation also affects overall reliability. As an example, the lifetime of transistors in a 65 nm CMOS technology was found to be only 0.2 year due to hot carrier damage when biased at a constant voltage bias condition.[1] It is obvious that comprehensive characterization of degradation effects is needed during the design phase of modern nanotechnology microelectronics circuits.

3 ProChek Reliability Characterization Instrument

Ridgetop Group provides a solution to this problem by providing an easily portable reliability testing platform that can be used as the standard test method by any IC design team.

Ridgetop has designed a portable and user-programmable process reliability evaluation system (ProChek) for CMOS and BiCMOS fabrication processes. The system can be used for accurate but still rapid and cost-effective qualification of the intrinsic reliability of CMOS and BiCMOS processes (including SiGe processes). The method uses a **Test Coupon** that is fabricated in multiproject wafer (MPW) shuttle runs in order to minimize the costs and expedite the qualification phase. The reliability qualification will be performed using measurement and data collection circuits in a **Benchtop System**, which connects to a **Test Card**, which in turn holds the Test Coupon. The Benchtop System is controlled by a **Host Controller**, which is a user-invoked graphical user interface (GUI) software application on a PC. Fabricated Test Cards and the Host Controller software are universal and can be used with Test Coupons from different fabrication runs. The Test Coupon is a standardized, all-digital structure and can be ported to different fabrication processes with minimum engineering cost.

This instrument eliminates the need for expensive test equipment in fabrication process reliability characterization, and it simultaneously provides a standardized platform for IC designers to perform the required reliability tests.

The four components of ProChek are shown in Figure 1.

[1]Silicon Blue 65LP Process Qualification Summary, v0.1, Silicon Blue Technologies, 2008, http://www.siliconbluetech.com/media/downloads/SBT_65LP_Process_Qual_v0.1.pdf

[2] Note that even if the Test Coupon has been designed to contain only easily portable digital logic, it can be used to characterize reliability

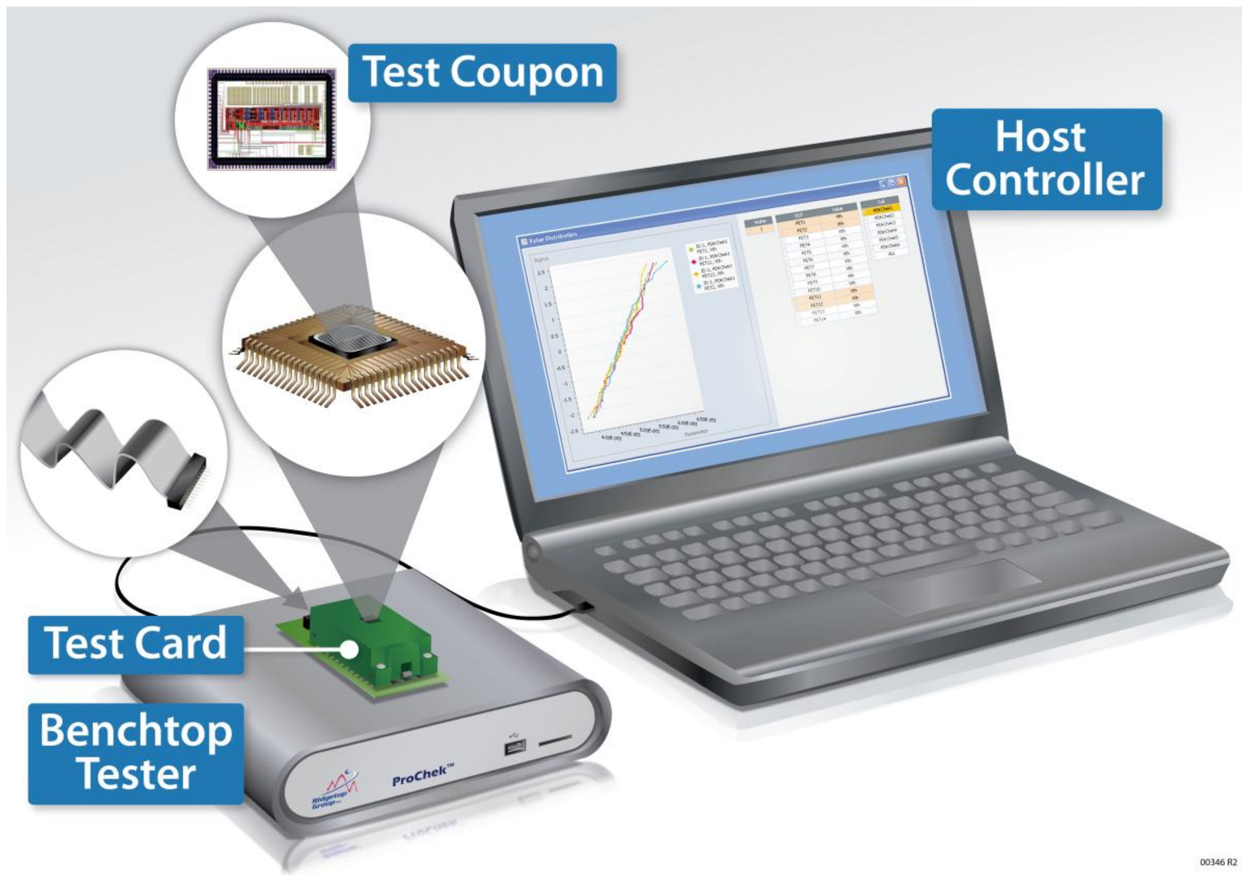

Figure 1: ProChek test system

In addition to the four-component structure shown in Figure 1, Ridgetop's ProChek supports a test flow in which the customers will use their own test equipment instead of using the Benchtop System. Ridgetop can provide the test structure IP and the result characterization software. The silicon area consumed by the test structure IP (Test Coupon) can be made smaller or larger, depending on the customer's requirements. The test structure block can even be made small enough (e.g., 300 µm X 300 µm) to easily fit on the same die with the actual IC, and it can then be used for reliability characterization of that die.

ProChek provides everything needed for fabrication process characterization for modern advanced transistor technologies. Moreover, if a tight development schedule puts constraints on the process characterization, the work can be outsourced to Ridgetop engineers.

3.1 Details of ProChek

Figure 2 is a more detailed illustration of Ridgetop's fabrication process reliability evaluation system (ProChek) which includes: Host Controller, which is a GUI application on a PC; Benchtop System, which consists of the main printed circuit board (PCB) and two daughterboards (these three boards are named MAIN BOARD, STRESS BOARD and MEASUREMENT BOARD); Test Card, comprising a socket containing the Test Coupon or with the Test Coupon directly attached, plus a connector to the underlying Benchtop Tester; and Test Coupon, which is a packaged silicon chip with arrays of test structures and which is placed on the TC BOARD. By using the GUI, the test structures can be

programmed to be subjected to highly accelerated test conditions that target all critical failure mechanisms of concern (TDDB, NBTI, etc.). Fabricated Test Cards and the Host Controller software are universal and can be used with Test Coupons from different fabrication runs.

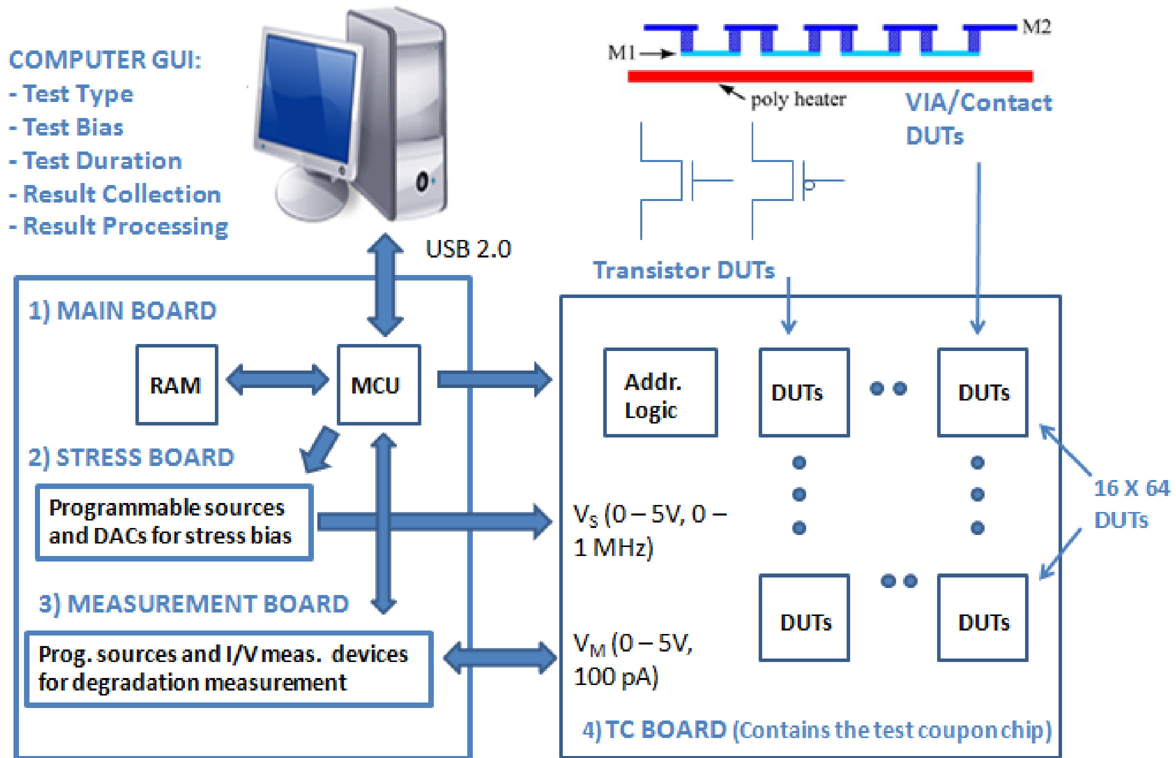

Figure 2: Structure of ProChek

3.1.1 Benchtop Tester

The reliability qualification is performed using measurement and data collection circuits on a common Test Card (this PCB is named MAIN BOARD in Figure 2), which holds two daughterboards (named STRESS BOARD and MEASUREMENT BOARD in Figure 2). These two daughterboards are used to perform the highly accelerated stressing and the degradation measurement functions, and they contain carefully selected commercial off-the-shelf (COTS) parts, such as programmable voltage sources, digital-to-analog converters (DACs), and Ridgetop's proprietary low-noise current monitors. The voltage measurement capability on the MEASUREMENT BOARD provides 500 ns measurement time and <5 µV accuracy, whereas the measurement time for the low current measurements is 10 µs with 3 pA accuracy and excellent repeatability.

3.1.2 Test Card

The Test Coupon chip (discussed in section 3.1.4) is placed on a daughterboard named Test Card in Figure 2. This daughterboard sits atop and is connected to the Benchtop Tester. The Test Card has a special test socket that allows the copper pad in the bottom of the package to be connected to a Peltier cooler for active cooling. Active cooling is needed to keep the package temperature within acceptable limits during the highly accelerated stress tests.

Note that Ridgetop's Test Card is designed for "highly parallelized package-level tests." Ridgetop's Test Coupon IP (discussed in section 3.1.4) can be used with wafer and die-level test setups as well, in which case much smaller leakage currents can be evaluated (down to 0.1 fA with Agilent's B1500A device analyzer).

3.1.3 Host Controller

The whole test system is controlled from the Host Controller, which is a software application on a PC. From the graphical user interface (GUI), the user can program test bias magnitudes and waveforms; test temperatures; and test durations. The GUI also collects the measurement results and processes them for better visibility of the failure effects. For example, the GUI has an algorithm that calculates threshold voltage (V_T) shifts from drain current measurements. Figure 3 shows a snapshot of a Ridgetop GUI that is used to control NBTI/V_T shift measurements.

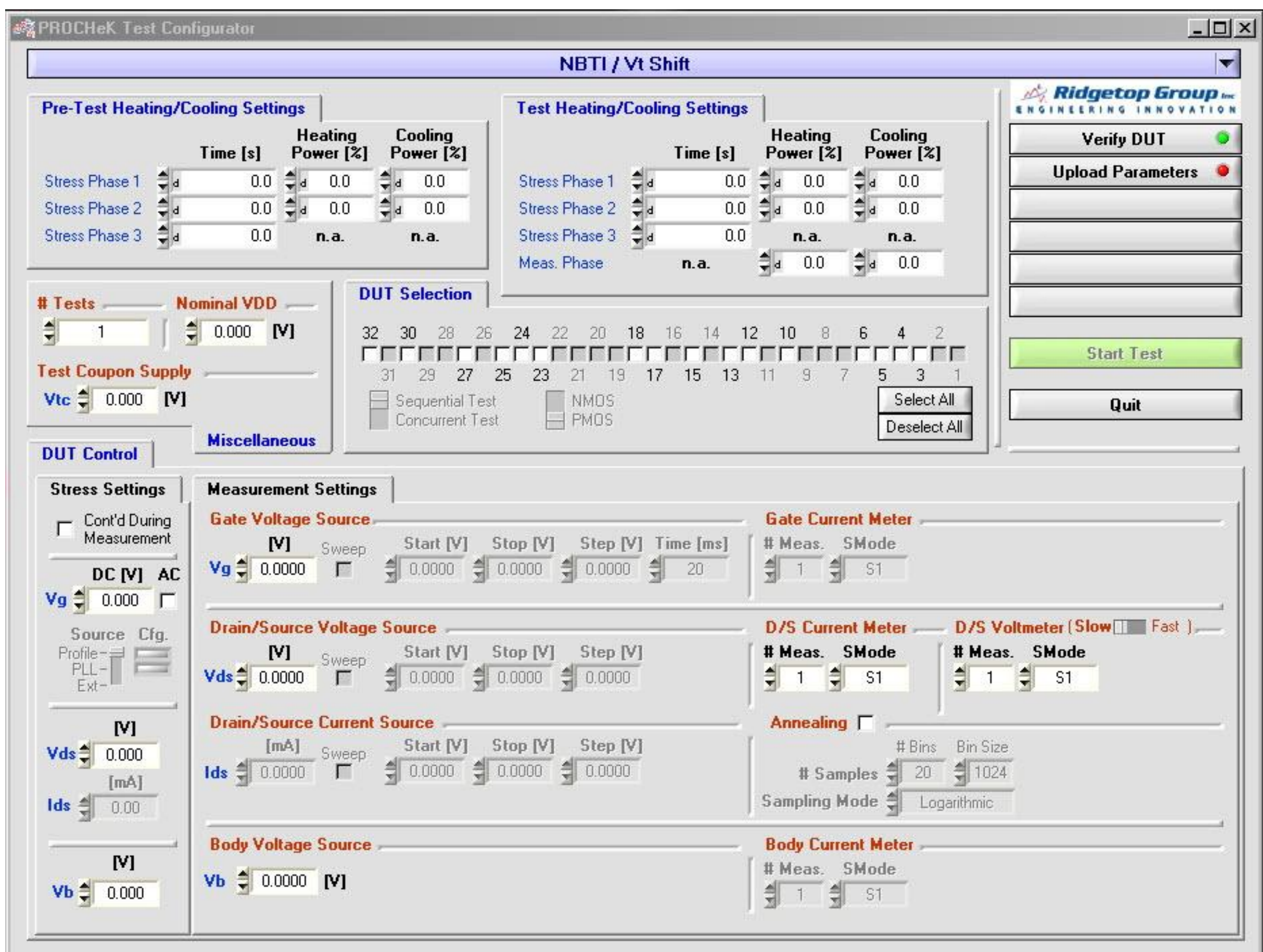

Figure 3: Screen shot of Host Controller software GUI for NBTI/V_T shift measurement

3.1.4 Test Coupon

The ProChek Test Coupon contains arrays of programmable test structures, as seen in Figure 2. The Test Coupon is a 1 mm^2 chip that is fabricated on a multiproject wafer (MPW) run and packaged in order to minimize the test costs and expedite the qualification phase. Ridgetop has selected an optimal high-reliability ceramic package for the Test Coupon. The current version of the Test Coupon has 16 arrays of 64 DUTs, and Test Coupons with more or fewer DUTs can be fabricated, if requested. Note that Test Coupons with fewer DUTs have a smaller layout area. Ridgetop has approximated that the minimum achievable silicon area that fits the Test Coupon, including all the required bonding pads, address logic, and a few hundred DUTs is 0.16 mm^2, when fabricated in a 45 nm CMOS process (e.g., 400 μm^2 with layout aspect ratio 1:1; other aspect ratios are possible).

The Test Coupon is a standardized, all-digital[2] architecture and can be ported to many different fabrication processes with minimum engineering cost. All of the control logic in the Test Coupon design can be synthesized from VHDL code and the DUTs are easily portable library files. The DUTS on the Test Coupon include: NMOS, PMOS and I/O transistors (different sizes); via and contact test structures; and radiation test structures.

3.1.4.1 Test Structures for Failure Effects

Highly accelerated stress tests targeting reliability concerns, such as negative bias temperature instability (NBTI), time-dependent dielectric breakdown (TDDB), stress-induced leakage current (SILC), hot carrier (HC) damage, electromigration (EM), and stress migration (SM) can be performed with ProChek. The degradation is significantly accelerated with the combination of stress voltages that are higher than VDD and high temperatures, created with localized, on-chip polyresistor heating elements. The tightly controlled heating capability can also be used to characterize the effect of varying operating temperatures on circuit reliability, which is of interest to engineers of modern high-density systems.

Both DC and AC[3] stress bias conditions can be programmed on the test units, which allows making accurate approximations of circuit lifetimes in realistic operation conditions. The ProChek system can also be used to evaluate the interactions between various aging effects, which may have unpredictable effects on circuit parameters.

The aging of individual transistors is dependent on the exact bias conditions it experiences during the operation, as well as global conditions such as temperature, which can have a significant gradient across the die. The transistor parameters also have a statistical variance due to process mismatches. Interestingly, the degradation of individual transistors also has a statistical variance of its own, i.e., two identical transistors under the exact same bias conditions and temperature will age differently. ProChek captures both effects; the variance due to process mismatches and the variance in different aging mechanisms, such as NBTI. Traditionally, the measurements needed to capture the statistical variation in aging processes are lengthy and expensive. Moreover, even if this data is measured by the manufacturer, only a limited amount of this data is made available outside the foundry.

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[2] Note that even if the Test Coupon has been designed to contain only easily portable digital logic, it can be used to characterize reliability problems that are concerns in both digital and analog circuits.
[3] In this reliability engineering context, DC and AC biases mean constant voltage bias and varying voltage bias, respectively.

The Test Coupon in ProChek includes large sample sizes of test structures, thus it provides very good statistical models for the physical effects that can be used as the basis of accurate aging simulation models.

To our knowledge, there are no other solutions currently available for rapid, low-cost reliability testing and aging parameter capture targeting nanotechnology ICs.

3.1.4.2 Acceleration of Circuit Degradation With Localized On-Chip Heating Elements

The required comprehensive reliability characterization work is very time-consuming and costly, partly due to the fact that the degradation mechanisms cannot be accelerated enough with currently existing methods. ProChek has innovative local heating elements that will shorten the test times by orders of magnitude, allowing very comprehensive evaluation within reasonable time and budget limits. The on-chip, tightly controlled heating capability can be also used to characterize the effect of varying operating temperatures on circuit reliability, which is of interest to engineers of modern high-density systems.

Similar local heating elements are commonly used in fast wafer level reliability (fWLR) testing. The reported data from fWLR tests shows that every 50 °C increase in the stress temperature will reduce the total test time by one order of magnitude in electromigration tests, as shown in Figure 4. Similar data have been reported for NBTI. This means that Ridgetop's local heating structures that can be used to heat the DUTs up to 325 °C shorten the required test times by several orders of magnitude compared to room temperature tests. This allows comprehensive process characterization within reasonable time and budget limits.

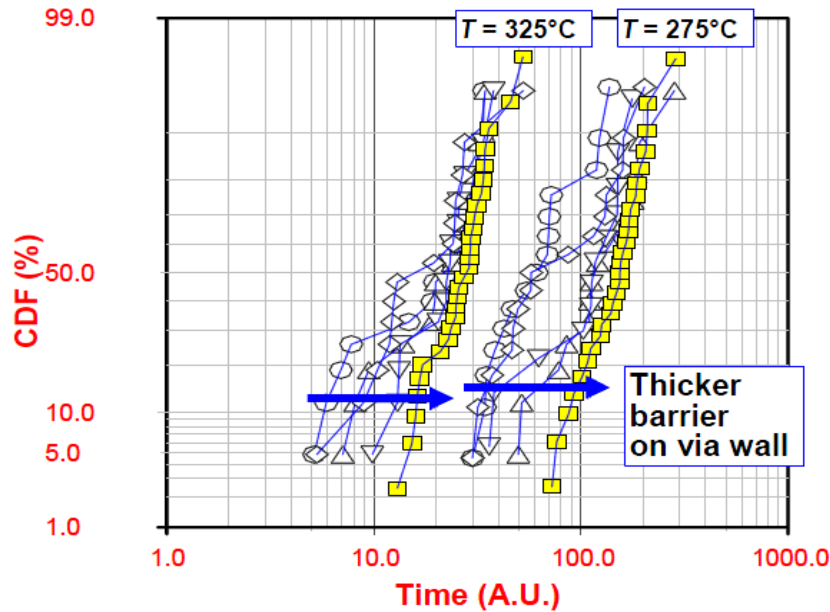

Figure 4: Reported data from fast wafer level reliability (fWLR) tests show that every 50 °C increase in the stress temperature will reduce the testing time by almost one order of magnitude[4]

Ridgetop has performed very careful, fully symmetrical layout design that includes dummy structures at the ends of the DUT arrays and other techniques to minimize any mismatch in the generated stress temperatures across the chip. Accurate temperature control is provided by on-chip diode-based temperature measurement circuits providing active feedback to the heater control structure on the test card.

Note that the user can set any stress temperatures between 25 and 325 °C from the GUI. Using the developed heating mechanism to significantly accelerate the aging is optional.

3.2 Benefits of ProChek

1. Provides rapid, low-cost reliability testing capability and aging parameter capture for advanced transistor technologies.
2. Considerably shortens the time needed for fabrication process reliability qualification.
3. Includes testing capability targeting all known important reliability concerns in nanotechnology (<90 nm) CMOS processes.
4. Provides much-needed reliability test data for advanced technologies, since only a limited amount of this type of data is made available outside the foundry.
5. Eliminates the need for expensive ATE equipment in fabrication process reliability characterization.
6. The Benchtop Tester provides a standardized, highly accurate measurement capability. Normally, the measurement setups at different facilities can cause significant

[4] Ki-Don Lee, et al., "Via Processing Effects on Electromigration in 65 nm Technology", 44th Annual International Reliability Physics Symposium, San Jose, 2006.

errors/deviations to the measurement results.[5] Every user of ProChek has the same standardized test setup, which eliminates these deviations. The evaluation software is standardized as well.

7. The Test Coupon in ProChek includes large sample sizes of test structures, thus it gives a very good statistical distribution for the physical effects that can be used as the basis of accurate aging simulation models.
8. Includes accurate measurement capability for process mismatch of most important design parameters, such as V_T and capacitance.
9. The on-chip, tightly controlled heating capability can be used to characterize the effect of varying operating temperatures on circuit reliability, which is of interest to designers of modern high density systems.
10. ProChek provides everything needed for advanced technology fabrication process characterization. Moreover, if a tight development schedule puts constraints on the process characterization, the work can be outsourced to Ridgetop engineers.

4 Ridgetop's Other Reliability Monitor Products and High-performance ICs

4.1 In-situ Reliability Monitors

Ridgetop has developed and optimized in-situ reliability monitors, i.e., Prognostic Cells™ over the last 10 years. They have shown to be very effective in giving early warning for fatal degradation levels due to NBTI, HCI, electromigration and TDDB, all of which are important reliability concerns for modern CMOS electronics. Ridgetop has also designed similar prognostic circuits for degradation effects in SiGe BiCMOS circuits. The time period from early warning to expected failure can be set by the mission requirements – it can be 18 months or six months, for example.

The reliability of integrated circuits during their operational life must be monitored and managed to ensure that the lifetime requirements are achieved. Reliability management encompasses identifying degrading lifetime in critical circuits and taking corrective action to extend the lifetime. Ridgetop's reliability monitoring and management concept incorporates acquiring the data, analyzing it, and modifying some aspect of the operating environment (voltage, temperature, clock rate, duty cycle, etc.). The processing and decision making could be done on-chip, on-board, remotely, or a combination of those.

Host circuits fabricated in CMOS, SOI, Bipolar or SiGe technologies can be monitored with Ridgetop's current set of Prognostic Cells. Ridgetop has extensive experience in the failure mechanisms of all these technologies and related precision test structure designs. The Prognostic Cell technology is based on setting the Prognostic Distance of the cells by a calculated amount of applied overstress, so that they will provide advance warning of an impending failure during operation (Figure 5).

Ridgetop has produced successful Prognostic Cells and process variation monitors in five different fabrication processes: NEC 90 nm, IBM 130 nm, TSMC 0.18 µm, AMI 0.5 µm, and Sandia 0.35 µm.

[5] Personal discussion with Ron C. Lacoe, a senior scientist from the Aerospace Corporation

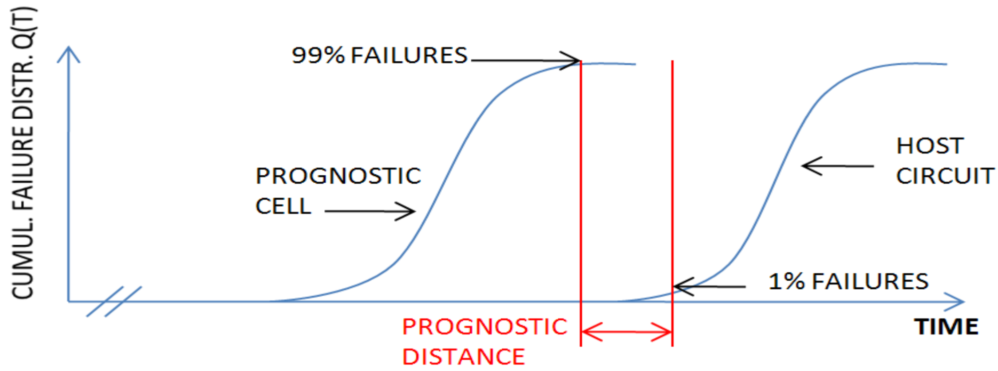

Figure 5: A Prognostic Cell is a sensor circuit that is designed to trigger a certain time period before an impending failure due to different types of degradation (NBTI, HCI, TDDB, electromigration, etc.); this time period is called "Prognostic Distance"

4.2 PDKChek™

Ridgetop's PDKChek measures die-level process-induced variations, both random and systematic, in MOS transistor threshold voltage (V_T), resistance, capacitance, and turn on/off current. PDKChek is an unobtrusive, stand-alone IP block designed to accurately and precisely measure the variation in parameters resulting from the randomness inherent in processing.

The PDKChek IP block provides circuit designers with independent verification data to improve the accuracy of process design margins, increase process yield, expedite problem resolution (design- or process-related), reduce design iterations (duration and frequency), and enable shorter time to market.

PDKChek allows for faster testing than traditional scribeline transistors. Testing can take place before or after packaging the die. Die-level testing takes advantage of test structures and bonding pads that are already present on the die, so there is no additional error introduced by the contact resistance of a probe station.

System-level implementation of PDKChek is shown in Figure 6.

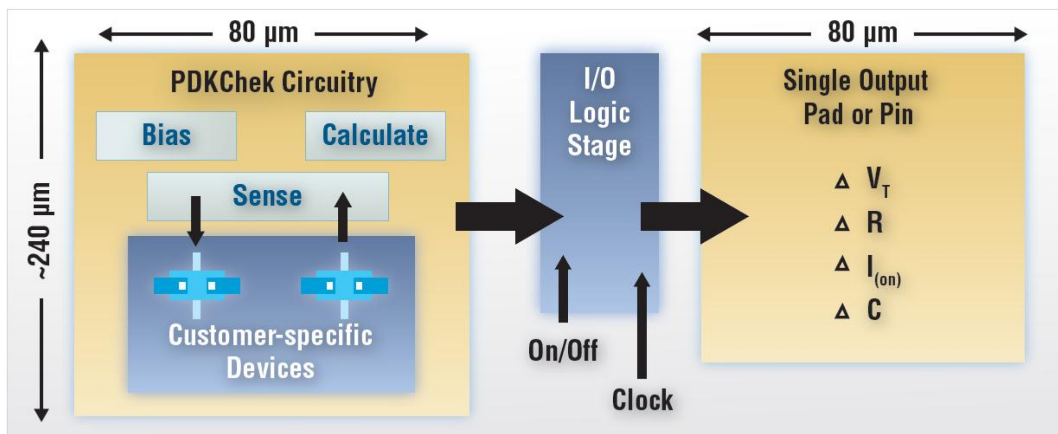

Figure 6: PDKChek system-level implementation

4.3 YieldMaxx™

The quick identification and correction of yield problems is an imperative issue that can be simply solved by YieldMaxx. Interfacing through an API with independent die-level process monitoring tools, YieldMaxx integrates large volumes of disparate data to provide accurate yield analysis in a matter of minutes. The user is able to correct the disparity faster due to an automated test equipment database.

The software analyzes and presents standard on-die, parametric data measurements of key performance parameters, such as threshold voltage, resistance, and capacitance. With a friendly GUI, YieldMaxx displays visual indications of device mismatch parameters, as shown in Figure 7.

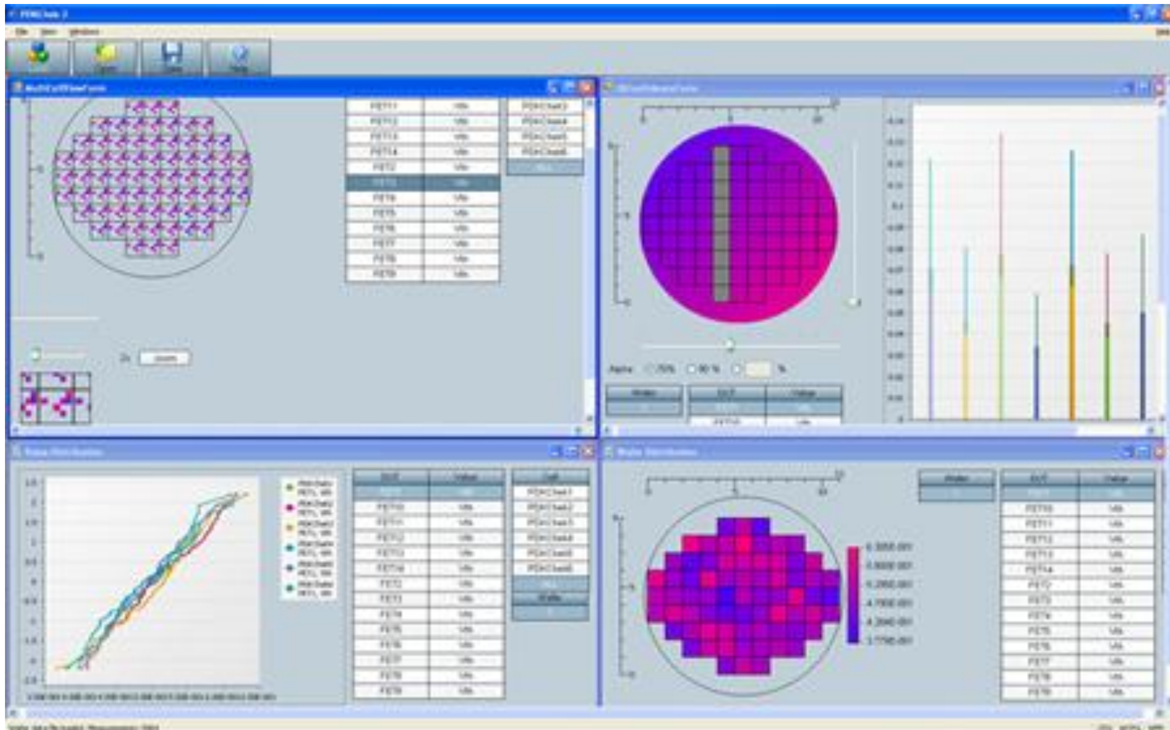

Figure 7: YieldMaxx graphical utility

4.4 Mixed-Signal ASICs

Ridgetop has a portfolio of high-performance ICs. These include a low-power 50 mW, 14-bit, 40 MSPS ADC and a built-in self-test (BIST) circuit that monitors degradation effects in ADCs. Ridgetop is currently designing a 12-bit, 500 MSPS, 470 mW ADC. Ridgetop has also been awarded a NASA contract to design a SiGe-based ADC for the Jupiter Europa Orbiter mission ice-penetrating radar. This ADC has the following specifications: 12-bit resolution, 125 MSPS sampling speed, 120 mW power dissipation, and it needs to be hardened to 5 Mrads of radiation.

5 Summary

Ridgetop's ProChek can be used for accurate, rapid, and low-cost fabrication process reliability characterization as a part of the IC design and qualification cycles. Providing an easy-to-use GUI with

data processing capabilities, universal test card, and portable test chip design IP, ProChek can be used as the standard reliability evaluation system among IC engineers.

Ridgetop has additional technologies that provide great benefits: Prognostic Cell, PDKChek, and YieldMaxx technologies, and a library of mixed-signal ASICs.

6 Company Information and Contacts

Ridgetop Group, Inc. is the world leader in electronic prognostics and reliability built-in self-testing (BIST). Ridgetop Group was founded in 2000 with the purpose of introducing revolutionary tools for electronic design. Headquartered in Tucson, Arizona, USA, Ridgetop Group develops families of intelligent design-for-manufacturing, BIST, and prognostic tools covering the entire semiconductor development lifecycle. Ridgetop also offers mixed-signal design and modeling services for critical applications and electronics in harsh environments.

Company Address:

Ridgetop Group, Inc.
3580 West Ina Road
Tucson, AZ 85741 USA
www.ridgetopgroup.com

Contact person:

Esko Mikkola, Ph.D.
Principal Engineer
520.742.3300
Esko.Mikkola@RidgetopGroup.com