Ridgetop Group Inc

ENGINEERING INNOVATION IN ELECTRONIC PROGNOSTICS

Semiconductor IP

Solder Joint BIST™ Test Platform Kit

Industry-Standard, High-Performance, Built-In Self-Test Technology

- Built-In Self-Test IP Core detects incipient fatigue damage to dedicated pins of FPGA packages, especially BGA packages
- Detects damage prior to catastrophic failure of FPGA
- Improves fault coverage without significantly increasing complexity of system
- Improves fault coverage for Advanced Redundancy Management without using redundancy techniques
- Provides positive correlation of hardware faults to intermittencies

General Description

The SJ BIST™ Test Platform Kit allows you to evaluate the SJ BIST (Solder Joint Built-In Self-Test) technology at a fraction of the cost of the IP core. The FPGAs are programmed to test 64 pins at various pin locations for a XILINX® FG 1156 FPGA. Additional boards are available upon request.

The SJ BIST™ Test Platform Kit (Figure 1) includes:

- A cable to connect each test board in the package to a National Instrument data acquisition board.
- Instructions on how to connect a test board to the card.
- A cable to connect each test board to a power supply with oscillator chip for an EPROM on each test board.

In addition, the following options are available for purchase:

Option 01: **A National Instruments LabVIEW™ program to control the collection of data from the FPGAs.**

Option 02: **A MATLAB® program to analyze the collected data.**

Option 03: **A power supply board for each test board.**

Figure 1: SJ BIST platform

Revision 1.0 (09-2009)

Background

Field Programmable Gate Arrays (FPGA) are used in more than 80% of new digital circuits; they are connected to the PCB with solder-joint ball grid arrays (BGA). The solder joints used in BGA assemblies in FPGAs are subject to cumulative fatigue damage, and the use of lead-free solder has further increased concern over BGA reliability.

To enable detection of incipient solder-joint fatigue damage in fine-pitch BGA assemblies – and thereby avoid catastrophic failure of the FPGA – Ridgetop Group has developed SJ BIST™ to monitor the condition of FPGA BGA solder joints. SJ BIST is programmed into the FPGA and a small capacitor is attached to selected, unused I/O pins to be monitored or prognostic-tested.

Prior to SJ BIST, there were no known methods for detecting high-resistance faults in functional solder-joint networks belonging to programmed FPGAs. SJ BIST is designed to detect occurrences of high-resistance spikes at BGA pins and to then alert the system regarding the condition of the solder joints. Maintenance is thereby facilitated, either through replacement or by switching to a redundant system prior to catastrophic failure.

Figure 2 illustrates the top view of the test platform kit.

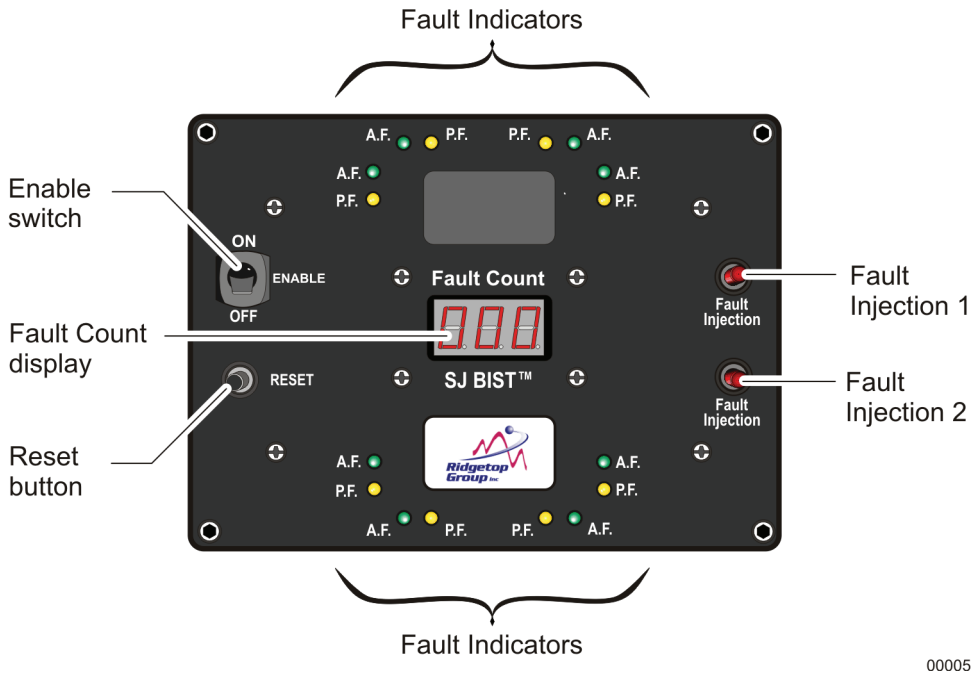

Figure 2: Top view of SJ BIST platform

Need modified or custom design? Contact Ridgetop at 520-742-3300 to discuss your ideal solution!

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