Ridgetop Group Inc
ENGINEERING INNOVATION

White Paper: Through-Silicon Via Interconnection Reliability Assurance System

1 Introduction

Ridgetop Group is developing a solution addressing the quality and reliability problems of applications that deploy “2.5D” and “3D” packaging technology for integrated circuits (ICs). Ridgetop’s research seeks to deploy a combination of innovative techniques for improved verification of the quality and reliability of 2.5/3D IC packaging and to provide prognostics so that related interconnect operational faults can be determined before actual failure occurs.

The 2.5/3D IC technologies employ through-silicon vias (TSVs), which enable greatly increased circuit density, performance, and functionality for a given volume. The 3D ICs stack directly on top of each other, with interconnections being made by matching bond areas and TSVs. The 2.5D ICs are similar, however they require the use of an interposer to route signals since the connection patterns of the TSV-enabled ICs do not directly correspond to the IC above or below. While these packaging solutions have the distinct advantages mentioned above over most other packaging/mounting technologies, there are disadvantages as well. The greater density leads directly to increased local heat, thus degradation and defects due to thermal effects are of great concern. Qualifying and testing such connections is very difficult and expensive, and techniques for anticipating failure do not currently exist. Confidence in the quality and reliability of 2.5/3D IC interconnects is therefore lacking. Systems that use them may require a high level of preventive maintenance whenever possible, or such packaging may simply be avoided when such maintenance is not possible or practical.

Ridgetop’s innovation will be the first to address the difficult issue of 2.5/3D IC package interconnect integrity after assembly is done and when the related devices are deployed in larger systems. The innovation will improve reliability of TSV-based packaging and provide prognostics so that interconnect-related operational faults can be determined before actual system failure occurs.

2 2.5/3D IC Integrity Testing Background

2.5D and 3D IC interconnect technology adoption has been increasing in recent years given its ability to increase the density of electronic circuitry that can be assembled in an IC package, which consequently helps to reduce required board space while also supporting higher operating frequencies due to shorter interconnects. While 2.5/3D IC interconnect technology has some distinct advantages over the traditional wire-bond attachment process and leaded packaging/interconnect technologies, implementation of this kind of interconnection scheme is much more complex, validation and verification is more difficult, and no solutions exist that allow validation of the connection integrity over time.

The state of the art today consists of combining static non-electrical optical and X-ray inspection with functional testing on assembled 2.5/3D IC packages. Extensions to the boundary-scan (structural) testing standards are being developed but are not yet deployed, and even then these solutions will not be adept at quality verification and reliability checking of interconnects once the packaged assembly is actually deployed in a larger system − nor will they focus on detecting intermittencies and performing dynamic integrity tests. Given the limited scope of existing test techniques, the electronics industry does not have high confidence in the reliability of 2.5/3D IC interconnects, and systems that use them face a high early lifetime failure rate that may require an elevated level of preventive maintenance that drives up overall costs.

3 Ridgetop's Technical Approach for 2.5/3D IC Integrity Testing

Ridgetop Group envisions innovative techniques that will greatly improve verifying the quality and reliability of 2.5/3D IC assembly and packaging technology, and it will in addition provide prognostics so that related interconnect operational faults can be determined before actual failure occurs. The techniques include:

- Adaptation and modification of Ridgetop's **SJ BIST**™ (Solder Joint Built-in Self-Test) technology (designed for prognostics of solder joint reliability for field programmable gate array (FPGA) chips in ball-grid arrays) for use in the 2.5/3D IC application environment. SJ BIST can detect connection marginalities due to mechanical, thermal, or electrical stress. Serving as a "canary in the coal mine," SJ BIST alerts the host system before actual failure occurs (and, of course, it also detects the failures when they do occur). Using SJ BIST will require modification to the way the intellectual property is packaged and deployed, and possibly some changes to the IP itself. SJ BIST is a capability unique to Ridgetop Group.
- Adaptation and modification of the high precision electrical current monitoring capability offered by our sister organization, Ridgetop Europe, to observe and report abnormal current flows that are indicative of malformed 2.5/3D IC connections and that are applicable to validating functional as well as power connections. Power connection verification is beyond the scope of boundary scan. Such pathological current signatures can be quite subtle and require sensitive instruments that are very close to the source of the problem. A current monitor may take the form of on-chip IP or an external instrument available via a test or auxiliary fixture. Examples of existing monitors are called **PG-Mon** (on-chip) and **QD-10xx** (external).

These technologies can be used during and following the 2.5/3D IC manufacturing process to validate the quality of the interconnect manufacturing process, to screen out defective or marginal devices from a connectivity perspective before they are deployed in target systems, as well as to instigate *in situ* testing after deployment to determine whether a connection fault has occurred – including intermittencies – or whether failure is likely to occur soon. Ridgetop Group

will extend SJ BIST and current-based monitors to detect marginal, faulty, and failed TSV interconnects.

Ridgetop will first validate the approach using both an external SJ BIST monitor (the IP will be embedded in a standard FPGA) and an external QD-10xx monitor. Both the FPGA and the QD-10xx will be mounted on a 2.5D IC interposer board and connected such that they can monitor critical TSVs. This will then support both static and dynamic detection of faulty interconnects in the 2.5D IC stack.

Then Ridgetop plans to embed the SJ BIST and PG-Mon monitors in a low-cost IC for mounting on the 2.5D IC interposer (Figure 1) as well as embedding the same (or similar) IP in otherwise standard 3D ICs, such that the TSV interconnect reliability monitoring can be validated for a full-fledged 3D IC stack (Figure 2).

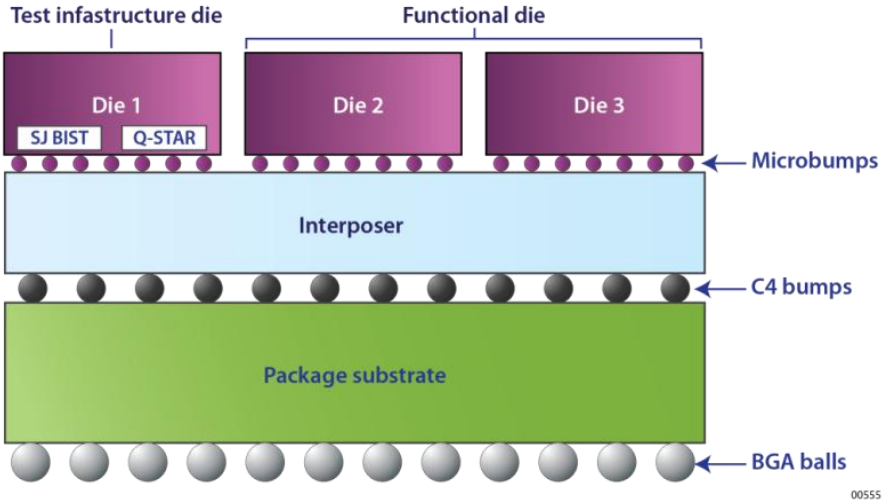

Figure 1: 2.5D IC Interconnection Reliability System with SJ BIST and Q-Star technology

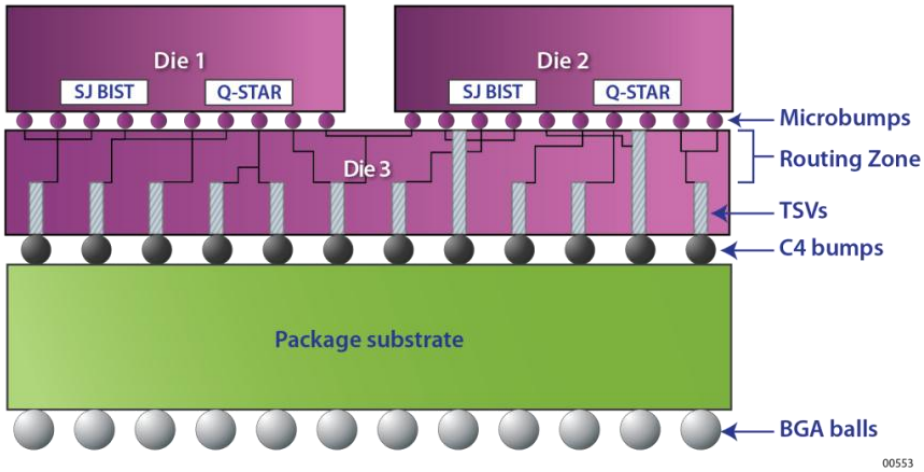

Figure 2: 3D IC Interconnection Reliability System with SJ BIST and Q-Star technology

In addition to the embedded instrumentation outlined above, Ridgetop will develop software to control and observe the embedded 2.5/3D IC reliability structures. This software, taking information from the embedded 2.5/3D IC reliability structures, will be able to run as a stand-

alone computer program. A related software program will be able to function as an embedded sentinel to alert the comprising system at large.

The requirements for such software will be identified first, then a prototype of an *in situ* software module that may be used to alert the host system of impending and actual failure will be developed.

To support widespread adoption, the design flow will also be addressed. Customers who adopt the techniques described above will be required to make small and straightforward changes to their 3D IC packaging design flow. They will need to instantiate the newly developed SJ BIST and/or PG-Mon IP into their chip and into the on-chip I_{DDX} current monitoring method. In addition, organizations that use 2.5D IC interposers will have the option of mounting a device on the interposer to host the SJ BIST and QD-10xx-derived IC. This will then support the functionality of monitoring the quality and reliability of a 2.5D IC interconnection without having to embed the IP in an IC elsewhere in their package. The 2.5D IC interconnection design flow methodology will be identified, then the design flow methodology for 3D IC packaging will be implemented. Ridgetop will also develop associated documentation and design support services to support the deployment of this solution to customers.

3.1 Technical Background

A number of techniques have been developed over the years to address the problem of interconnect testing, such as boundary scan, X-ray and optical inspection techniques. These techniques are primarily focusing on answering the question: “Is the interconnect present?” but do not answer the question “Is the interconnect reliable?” and do not always allow making a quality assessment of the interconnect. They also focus on functional interconnects and typically ignore power and ground connections.

None of these techniques provides reliability-related information or is able to identify a defective connection out of a group of parallel connections. Being able to validate all of the device's pin connections becomes more important, as the number of device pins as well as the number of supply pins increase drastically with the further miniaturization of IC technologies and the pin dimensions of the packages.

With X-ray laminography, all pins, including power and grounds, can be inspected for opens as well as marginal opens at the printed circuit board (PCB) level. Typically 98% of all solder joints on a PCB can be inspected. However, an X-ray test cannot check the electrical properties of the joint and does not support continuity tests, and applicability to 2.5/3D integration technologies is constrained.

Analog harmonic tests, RF induction, and analog junction techniques enable verification of the electrical properties of the connection (detection of opens and partial opens) but they require a time-consuming learning phase and are not able to diagnose highly parallel connections. They also are not applicable for embedded connections and have limited applicability for 2.5/3D integration technologies.

An overview of some of these main approaches follows.

3.1.1 Boundary Scan

Boundary scan is a standardized approach (IEEE Standard 1149.x, P1500, ...) resulting from work done by the Joint Test Action Group (JTAG) to enhance PCB and in-system testing by overcoming the technological limits of bed-of-nail fixtures due to ever-increasing miniaturization of PCBs and the ever-increasing complexity of the components being used.

The boundary scan test technology is an approach initially aiming at improving PCB testing by providing access to the input and output (I/O) pins of complex circuits on a PCB by means of a 4-wire test bus. Boundary scan also aims at reducing the time to design tests using traditional design methodologies and automated test equipment (ATE). The initial target was to support interconnect testing and in-circuit testing (as a replacement for the bed-of-nails approach) by extending IC test principles to the board level and eventually to the system level. Boundary scan evolved into many other applications as well, as illustrated in Figure 3.

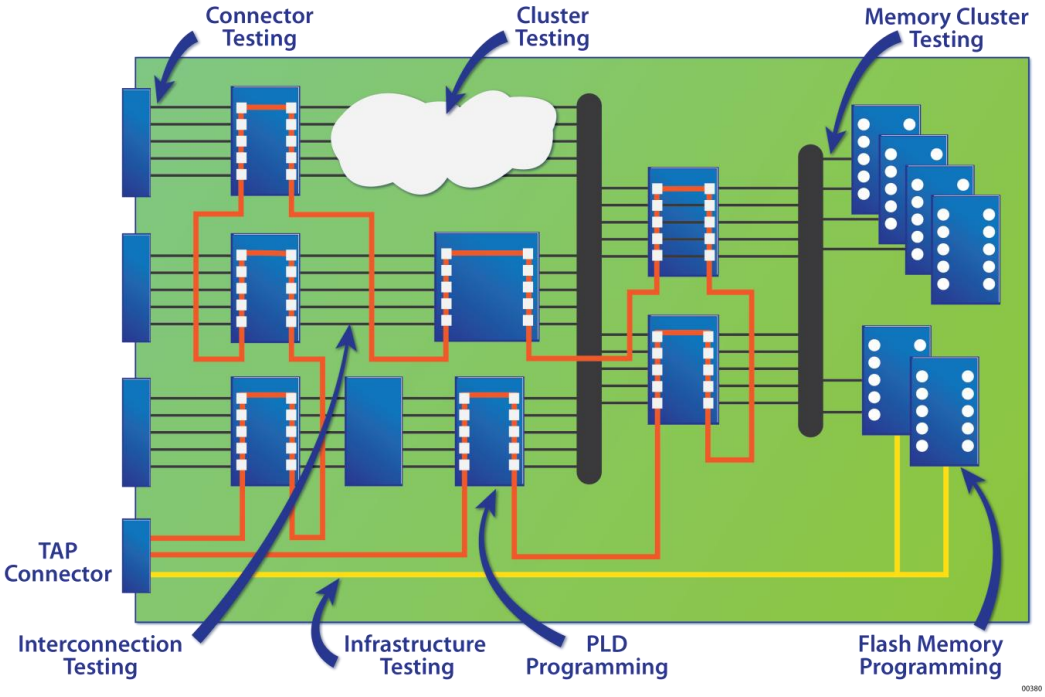

Figure 3: Boundary scan technology

With focus on interconnect testing, boundary scan has the following capabilities and limitations:

Boundary Scan Concept

A specific pattern is applied to the I/O pins of the "sender," the pattern is read at the I/O of the "receiver," and a match is done between the applied and received pattern as part of decision making. Applying and reading the patterns is done by shifting the data through the boundary scan chain under control of external test equipment connected to the test access port (TAP) connector.

Boundary Scan Pros & Cons

- Functional interconnects between two devices can be tested, provided both devices have boundary scan functionality (sender and receiver have to be boundary scan-enabled).
- Only applicable to functional interconnects (not applicable to power/ground pins).
- Requires a separate test mode operation to validate the interconnect (not applicable during normal functional operation).
- Can only provide info on whether there is a low resistive connection path.
- High resistive connections may escape detection.
- No info on degrading and degraded connections, no info on interconnect resistance.

- Requires additional (external) control for test (to apply the test conditions and capture responses) and verification (to match received responses with expected responses).

3.1.2 Ridgetop Group's SJ BIST Technology

SJ BIST is technology that was initially developed by Ridgetop to ascertain interconnection integrity for FPGAs in ball-grid array (BGA) packages. It focuses on interconnect reliability observation and analysis during the product lifetime. The SJ BIST IP embedded into a chip can be used both as an initial interconnect reliability test and as an in-situ monitor once the IC that embeds SJ BIST is deployed in its application, as shown in Figure 2.

Solder joints are subject to mechanical failure; they inevitably suffer damage from thermal and vibrational stresses, causing troublesome intermittent connections between components on the boards. The ability to measure, detect, and predict solder aging and the resultant failure of electronic modules is a true advancement in electronics reliability.

SJ BIST can detect connection marginalities, such as those caused by mechanical or electrical stress. Serving as a "canary in the coal mine," SJ BIST alerts the embedding system before actual failure (and also detects actual failures). Furthermore, SJ BIST detects solder-joint connectivity faults with a high degree of sensitivity and resolution: it is capable of reliably detecting temporary interconnect resistance increases of 100 ohms or more only occurring for tens of nanoseconds whereas traditional (boundary scan) approaches are only able to detect MΩ range increases that last at least for hundreds of nanoseconds.

Figure 4 illustrates the SJ BIST operating principle that is based on treating the interconnect as a memory (represented by a capacitor), and evaluates how interconnect properties affect reading and writing information in the memory (represented by charging/discharging the capacitor).

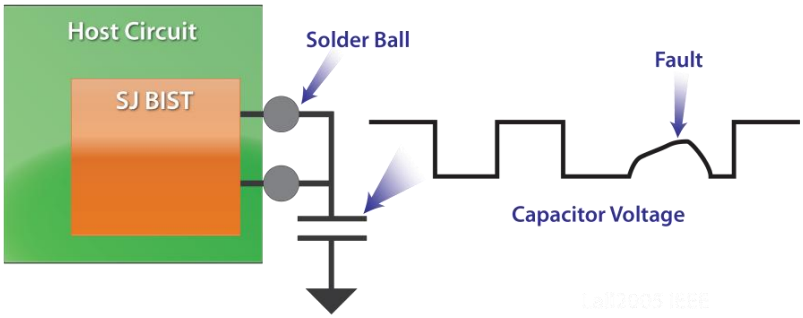

Figure 4: SJ BIST monitoring FPGA-to-board solder connection

With focus on interconnect testing, SJ BIST has the following capabilities and limitations.

3.1.2.1 SJ BIST Concept

The SJ BIST concept is based on creating a "connection loop" using dedicated device I/O pins and observing the amount of charge that can be transferred over a predefined time period.

3.1.2.2 SJ BIST Pros & Cons

SJ BIST:

- Requires well-selected and dedicated I/O pins (I/O pins occupied by SJ BIST cannot be used for other purposes).

- Cannot (at present) coexist with functional I/O.
- Allows concurrent observation (SJ BIST observation can run concurrently with normal system operation).
- Can only provide info related to the dedicated pins/contacts it is monitoring.
- Can identify/distinguish between good – degraded – bad connections.

3.1.3 Q-Star Test QD-10xx and PG-Mon

The ability of Ridgetop Europe's Q-Star Test instruments to make precision measurements is unmatched, and more than 750 instruments have been installed for specialized I_{DDX} semiconductor measurement applications at more than 70 different locations.

3.1.3.1 QD-10xx

The QD-10xx family of precision current monitors encompasses simple and full-featured, advanced configurable quiescent supply (I_{DDQ}) and ground (I_{SSQ}) current measurement instruments, supporting both probe and final test applications. As add-on instruments they extend the capabilities of existing test equipment, make current testing practically viable, and easily support a wide range of I_{DDQ}/I_{SSQ} test and measurements applications. They have on-board memory and data processing capabilities and provide digital measurement values as well as pass/fail information.

QD-10xx Concept

The QD-10xx instruments operate according to the stabilized voltage drop principle and are designed to be inserted in the path of which the current is to be measured unobtrusively so that no voltage droop is induced by the instrument and that the measured current is not altered by the instrument's presence. The units can drive high capacitive loads (up to several µF)**.** The QD-10xx products offer the capability to perform accurate (down to pA), high resolution (16- or 24-bit) and highly repeatable high speed (up to 10 kHz) static current measurements in combination with a wide dynamic measurement range. On-board data processing allows improving the accuracy further at the cost of a small speed penalty.

QD-10xx Pros & Cons

- Rather complex mixed-mode circuit.
- Virtually transparent, no induced voltage droop.
- Enables reliable and repeatable detection of subtle variations.
- Very high precision combined with a very short measurement time.
- Highly repeatable operation.
- On-board data processing and decision making.

3.1.3.2 PG-Mon

PG-Mon technology was initially developed to ascertain interconnection reliability for power and ground connections, as a solution to the problem of verifying that *each individual* connection out of the set of parallel connections that make up a power or ground connection, required to assure proper power distribution to today's complex designs, has a proper and reliable connection. PG-Mon is a non-invasive, highly reliable, testable and (boundary) scan-controllable on-chip CMOS current sensor, suited for the validation of IC and module connections and its application at the system-on-chip (SOC), board, and system level.

PG-Mon is not only an alternative to other techniques such as optical, X-ray and other inspection techniques, it is also an extension. The monitor exploits the inherent resistance of the connection under test. It is designed to be fully transparent, testable, and guarantees a proper detection, irrespective of local and global process parameter variations thereby avoiding the need for calibration. It can also be put in a power-down mode.

Verifying the continuity of a supply pin is easy when only one power and ground pin is used to supply a circuit, as a connectivity problem will result in a functional or timing failure. The situation is different when a circuit is supplied through multiple power and ground pins. Verifying whether each of these connections is made properly is difficult, as they are mostly connected in parallel, forming the IC's power distribution network. A failure of one of them initially will only marginally affect the global connection characteristics, also take into account potential pin redundancy. It is very difficult to measure globally as the variations caused by a failing connection will be masked by normal process parameter variation. However, such a problem will affect circuit and system operation, performance and reliability, especially when designers cannot afford as many power pins as required to have adequate margins.

Deep submicron and nanotechnology designs show an increasing dependency on high quality low impedance power supply networks. As a result, the amount of power connections is bound to explode with respect to the number of data pins for future-generation ICs. Multiple power ground pin connections cannot be tested easily once the IC is mounted in a package.

PG-Mon thus (1) checks individual connections that are part of a parallel connection, (2) checks connection integrity (whether the connection is present or not), and (3) checks healthiness/reliability of a connection (whether the resistance of the connection is below a certain threshold). PG-Mon is self-contained (no external instrumentation needed) and requires only a trigger to perform its action. It can easily be integrated into a BIST scheme.

PG-Mon Concept

The PG-Mon circuitry consists of a small switchable current sink and observation circuitry. The decision is based on two observations: (1) the current sink is switched out and PG-Mon samples the base situation, and (2) the current sink is switched in, causing a known additional current to flow through the connection under test. PG-Mon makes its decision based on comparing the two observations and can be tuned (by design) for specific trigger points. If the connection is good and reliable, then most (or all) of the current drawn by the sink will flow through the connection under test. If the connection is degraded then the amount of current flowing through the connection under test will either degrade as well (when observing parallel connections) or cause a higher voltage droop (higher resistance of the connection), affecting the decision making. Figure 5 illustrates the PG-Mon concept.

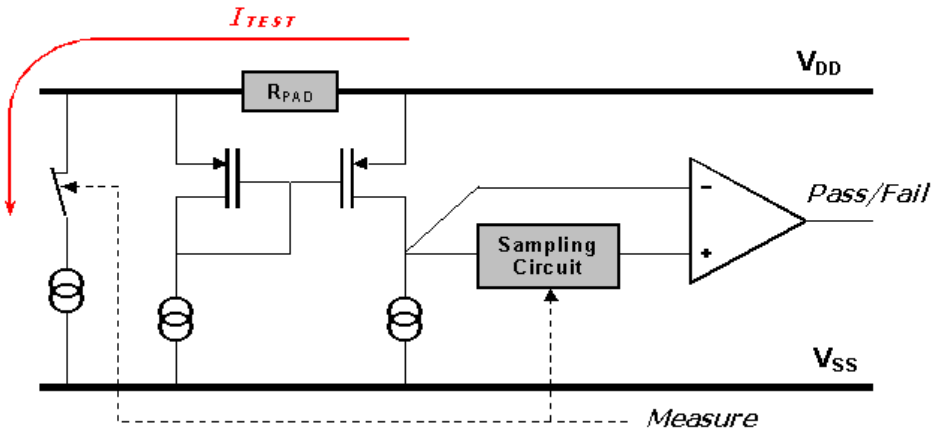

Figure 5: PG-Mon concept and simplified schematic

PG-Mon Pros & Cons

PG-Mon:

- Can be applied to any connection.
- Does not affect I/O performance.
- Requires a small current source/sink attached to each connection to be tested that is activated during the test mode.
- A PG-Mon core is needed for each connection that needs to be checked.
- Can provide info on all pins observed; the basic requirement is that a current path can be established.
- Original concept requires normal mode operation and test mode operation.
- Concept can be adapted to use observation of normal current rather than test current.
- Concept can be adapted so that its basic observation runs concurrently with normal operation.
- Needs to be designed-in.

4 Anticipated Benefits

The anticipated benefits are smaller and better electronic products with more reliable operation, yielding less waste and customer returns, higher system uptimes and lower system downtimes, and more efficient problem diagnosis, all contributing to more energy efficient applications and a greener world.

The cost to fix a problem grows by a factor of 10 for each successive stage of an entity's life cycle. The 2.5/3D ICs go through manufacturing, packaging, assembly, and deployment stages. A finished system that fails because of an unreliable TSV can lead to the loss of millions of dollars, but failures at even earlier stages can be quite expensive to detect, diagnose, isolate, and repair. This technology can be applied to 2.5/3D ICs at each of these stages and can result in tremendous savings for agencies and companies. The cost to implement this technology – adding a small amount of circuitry to each 2.5/3D IC – is insignificant when compared with the potential losses if this technology is not deployed.

5 2.5/3D Market Opportunity

As electronic devices are becoming smaller and more complex, limited area for circuitry has become a challenge for manufacturers. Thus, the semiconductor industry has started to address that challenge by making 2.5D ICs to ultimately reach the goal of making 3D ICs.[1] Some of the motivations for 2.5D/3D IC technologies are reductions in wire area and more power density, which are achieved by the TSV interconnects. This technology provides great benefits such as better performance, lower power, mixed die technologies, and smaller form factor.[2]

While 2.5D/3D IC technology increases performance by over 145%,[3] several challenges are yet to be overcome in order to reduce costs and increase efficiency. These challenges are mainly presented in areas such as yield, heat, testing, lack of standards, among others.[4] Yield problems are generally present due to additional steps in manufacturing of TSV-based 3D ICs. Another major challenge is testing, which is crucial to increase yield and improve cost efficiencies. Conventional testing methods do not meet the needs for accurate 3D IC testing, which are critical for a wider adoption of this technology. Thus, Ridgetop sees a great opportunity for this technology in the 2.5D/3D IC market, since it provides improved technologies to ensure reliability of 2.5D/3D IC packaging by predicting interconnection failure before it occurs. Other adoption barriers include supply chain issues, lack of design tools, and lack of standardized manufacturing processes.[5]

The competitive advantage of this technology is the combination of boundary scan and built-in self-test (BIST) capabilities. This allows verification of the integrity of the interconnects between integrated circuits while having an in-situ prediction capability to detect interconnects' impending failures.

6 Conclusion

Ridgetop's technology represents an attractive and innovative capability to provide accurate testing and prognostics of impending failure for interconnections in 2.5D/3D ICs. The industry is in need of effective testing tools that support increased chip reliability. The ultimate goal for the market is to overcome production and testing challenges.[6]

Traditional techniques for testing ICs are not effective for emerging technologies such as TSV or 3D ICs. The lack of accurate testing techniques represents a reliability risk. Thus, Ridgetop sees a great opportunity in this market for providing new capabilities leading to DFT, and interconnects in-situ testing and prediction of failure.

Customers will be able to design and fabricate chips intended for 2.5/3D IC packaging with this technology embedded on each die or on interposer boards. By allowing customers to assure themselves – both during manufacturing test and following end-use deployment – that the

[1] Bolsens, Ivo. "2.5-D will be a market of its own." EE Times. 2012. http://www.eetimes.com/design/eda-design/4236772/2-5-D-will-be-a-market-of-its-own-.
[2] GSA Memory conference, "3D-IC Challenges," Mentor Graphics, 2011.
[3] Krishna C. Saraswat, K. Banerjee, A. R. Joshi, P. Kalavade, P. Kapur and S. J. Souri, "3-D ICs: Motivation, Performance Analysis, and Technology".
http://www.google.com/url?sa=t&rct=j&q=&esrc=s&source=web&cd=3&ved=0CDsQFjAC&url=http%3A%2F%2Fciteseerx.ist.psu.edu%2Fviewdoc%2Fdownload%3Fdoi%3D10.1.1.23.3041%26rep%3Drep1%26type%3Dpdf&ei=hWt4UNSeEfGgyAGEi4D4DA&usg=AFQjCNEWzJXHDTdJu2fHSladTfvLunO3TA
[4] Wikipedia. "Three-dimensional integrated circuit." Wikipedia. 2011. http://en.wikipedia.org/wiki/Three-dimensional_integrated_circuit.
[5] Global Industry Analysts, Inc. "Global 3D Chips/3D IC Market to Reach US$5.2 Billion by 2015." PRWeb. 2012. http://www.prweb.com/releases/3D_chips/3D_IC/prweb4400904.htm.
[6] Global Industry Analysts, Inc. "Global 3D Chips/3D IC Market to Reach US$5.2 Billion by 2015." PRWeb. 2012. http://www.prweb.com/releases/3D_chips/3D_IC/prweb4400904.htm.

internal interconnections within 2.5/3D IC packages are reliable, companies and organizations will increase the adoption of 2.5/3D IC packaging technology in the targeted areas such as electronic sensors for high energy physics experimentation equipment, power grid applications, and others demanding an optimal combination of performance, power, reliability, compactness, and cost. Beyond simply saving time and money, by eliminating unreliable 2.5/3D IC packages from inclusion in end systems, customers will be able to determine impending failures in real time *after deployment* and take mitigating actions to avoid mission or application failure. This project ultimately leads to clear economic and technical advantages for 2.5/3D IC vendors and users.

7 Company Information and Contacts

Ridgetop Group, Inc. is a world leader in electronic prognostics and reliability BIST. Ridgetop Group was founded in 2000 with the purpose of introducing revolutionary tools for electronic design. Headquartered in Tucson, Arizona, USA, Ridgetop Group develops families of intelligent design-for-manufacturing, BIST, and prognostic tools covering the entire semiconductor development lifecycle. Ridgetop also offers mixed-signal design and modeling services for critical applications and electronics in harsh environments.

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