Contemporary Design for Testability Guidelines for Circuit Boards and Systems

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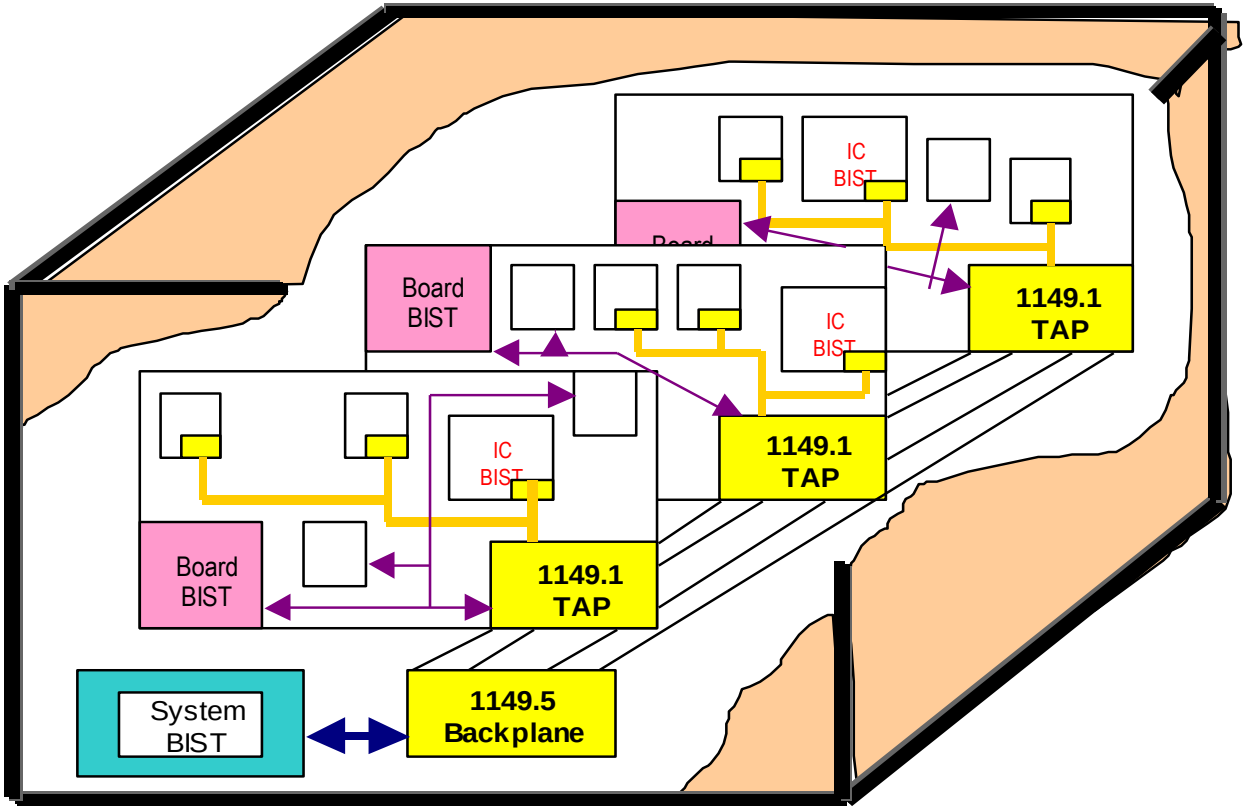
December 10, 2014

Contemporary Design for Testability Guidelines for Circuit Boards and Systems

Presented by: Louis Y. Ungar

Sponsored by Ridgetop Group Inc., December 10, 2014



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About the Presenter and Advanced Test Engineering (A.T.E.) Solutions, Inc.

Louis Y. Ungar

Position – President of A.T.E. Solutions, Inc., the leading testability consulting and educational firm

Professional Associations – President of the Testability Management Action Group (TMAG), Consultant to the American Society of Test Engineers (ASTE), SMTA Testability Committee, Member of the IEEE and IEEE Standards Balloting Committee for IEEE-1149.1-2013 & IEEE-1687.

Major Accomplishments – Educated nearly 10,000 test professionals from 2 dozen countries, consulted more than 100 organizations, created BestTest information source for test professionals, patents for Built-In Self Test, worked on DFT standards for SMTA, IEEE, IPC. Created The Test Flow Simulator and The Testability Director, software packages…

Education – BS in Electronics Engineering and Computer Sciences from UCLA, completed course work for MA in Management

Professional Goals – Convince engineers and managers that product quality through better test is not only noble, but also cost-effective

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Webinar Content

- What is DFT and Why We Need It?
- Guidelines and Standards for DFT and BIT
  - Military standards and guidelines
  - IEEE standards for boundary scan (JTAG)
  - Professional Society Guidelines
  - Commercial Company Guidelines
- New standards and guidelines
- New and coming technologies and solutions

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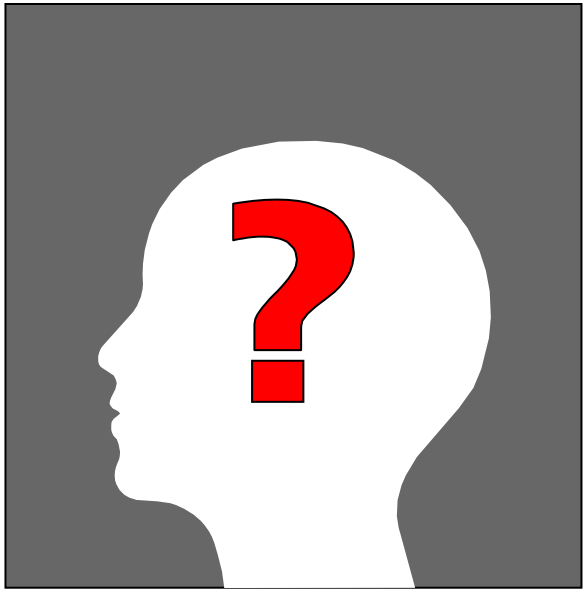
WHAT IS DESIGN FOR TESTABILITY?

- **Design for Testability is a philosophy incorporated in the design of electronic circuits which takes into consideration the post-design testing phase, and which attempts to reduce the effort and cost of testing.**



Testability = Controllability + Observability

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MOTIVATIONS FOR TESTABLE DESIGNS

- Reduce Test And Support Costs
- Gain Higher Product Quality Through Better Test
- Test Earlier And Improve Time To Market

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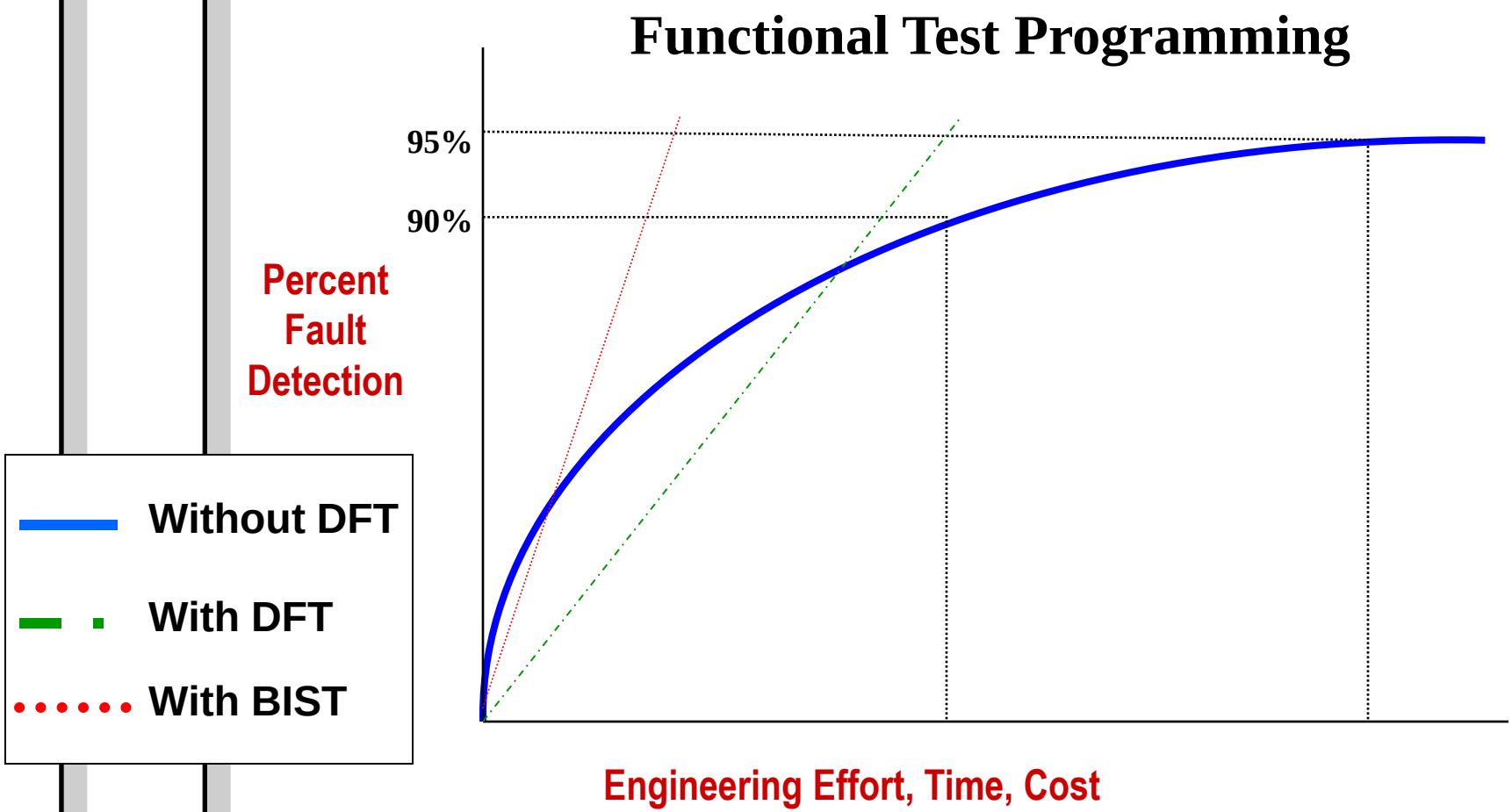
Test Programming
The Greatest Cost of Test



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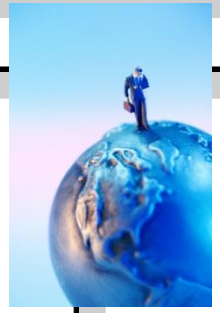
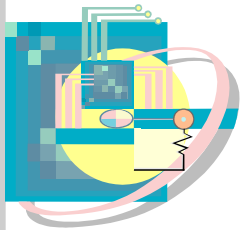
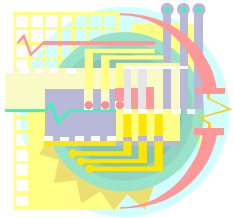
The Most Important Testability Guidelines:
When DFT Analysis is Performed and by Whom?



- **When?**
  - At conceptual design stage
  - During preliminary design stage
    - » Block diagram
  - Several times during detailed design and before design release





- **Who?**
  - DFT Analysis can be performed by designers, test engineers and testability engineers.
  - Trade-off analyses between various options should involve management.
  - Actual design changes must be made by designers

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DFT Guidelines and Standards

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Design for Testability Guidelines and Standards

- Military Standards, Guidelines and Handbook
- IEEE Standards with Boundary Scan
- SMTA/TMAG Testability Guidelines
  - Including probing and fixturing guidelines as well as "inspectability" for Automatic Optical Inspection and X-ray
- Commercial Guidelines
  - For sale software and free guidelines from tool makers
- IPC Design for Excellence (DFX) Guidelines
- Emerging and Future Efforts

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Design for Testability Guidelines and Standards

- **Military Standards, Guidelines and Handbook**
  - **FMECA - Procedures for Performing a Failure Mode Effects and Criticality Analysis MIL-STD-1629A Nov 1980**
  - **Testability Standard MIL-STD 2165 Testability Program Electronic Systems of 1985 became MIL-HDBK-2165 July 1995**
  - **US Navy Technical Brief ABM 1001-01 Oct 2001 Best Practices in Built-In Test**
- **IEEE Standards with Boundary Scan**
- **SMTA/TMAG Testability Guidelines**
- **Commercial Guidelines**
- **IPC Design for Excellence Guidelines**
- **Emerging and Future Efforts**

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MIL-STD-1629A FME[C]A and Testability

- FMEA is a great input to DFT – Due early in design
- FMEA provides important bases for Testability
  - The number of failure modes identified provides a scope of how large the test will be
  - Each failure mode that has an effect implies detectability
    - » No effect implies testability problem
  - Multiple effects for a failure mode imply diagnosis issues
    - » A single effect for a failure mode means perfect diagnosis
  - Reliability and failure rate information in FMEA provides reliability weighting for both fault detection and isolation
- IT IS CRUCIAL THAT FMEA BE PERFORMED EARLY IN THE DESIGN!

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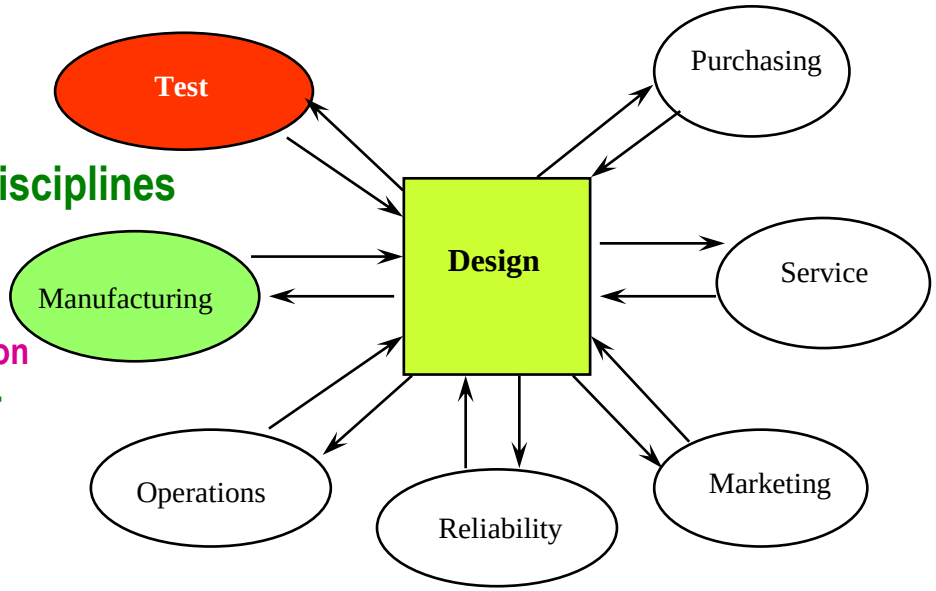
MIL-HDBK-2165 Testability Standard

Includes:



DEFINITIONS AND ACRONYMS
– to help communicate across disciplines

- PER MIL-STD-1309C
- Detail Requirements
- Test Descriptions and integration

Task Selection – to manage DFT

- Task 100- Program monitoring and control
- Task 200- Design and Analysis
- Task 300- Test and Evaluation

Appendix A - Testability program application guidance

Appendix B- Inherent Testability Assessment – criteria in question form

- Weighting and scoring different guidelines by designers and test engineers

Appendix C - Glossary

US Navy Technical Brief ABM 1001-01

Built-In Test Design and Optimization Guidelines

- **Purpose**

  To identify best practices in management, design and test in order to improve the reliability of fielded Built-In-Test (BIT) capabilities

- **Scope of BIT**

  Provides "built in" monitoring, fault detection and isolation capabilities as integral features of the system design.

  BIT uses internal system hardware and software to test the system or its subsystems.

  It often uses internal microprocessors and self-test software to isolate failures.

  It can be supplemented with embedded "expert system" technology that incorporates diagnostic logic into the prime system.

  - » These supplemental capabilities should be used to address specific BIT deficiencies that cannot be effectively addressed via other means.

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Design for Testability Guidelines and Standards

- Military Standards, Guidelines and Handbook
- **IEEE Standards with Boundary Scan**
  - 1149.1 Digital Boundary Scan
  - 1149.4 Mixed Signal Boundary Scan
  - 1149.5 System Level Boundary Scan - **Dropped**
  - 1149.6 Boundary Scan for Differential and AC Coupled Circuits
  - 1149.7 2-pin Boundary Scan and Bulk Data Transfer
  - 1500 Embedded Cores Accessed via Boundary Scan
  - 1532 Boundary Scan to program on-board programmable devices
  - 1581 Interconnects Boundary Scan with memory and provides protocol
  - 1687 Transports results of embedded test via Boundary Scan
- SMTA/TMAG Testability Guidelines
- Commercial Guidelines
- IPC Design for Excellence (DFX) Guidelines
- Emerging and Future Efforts

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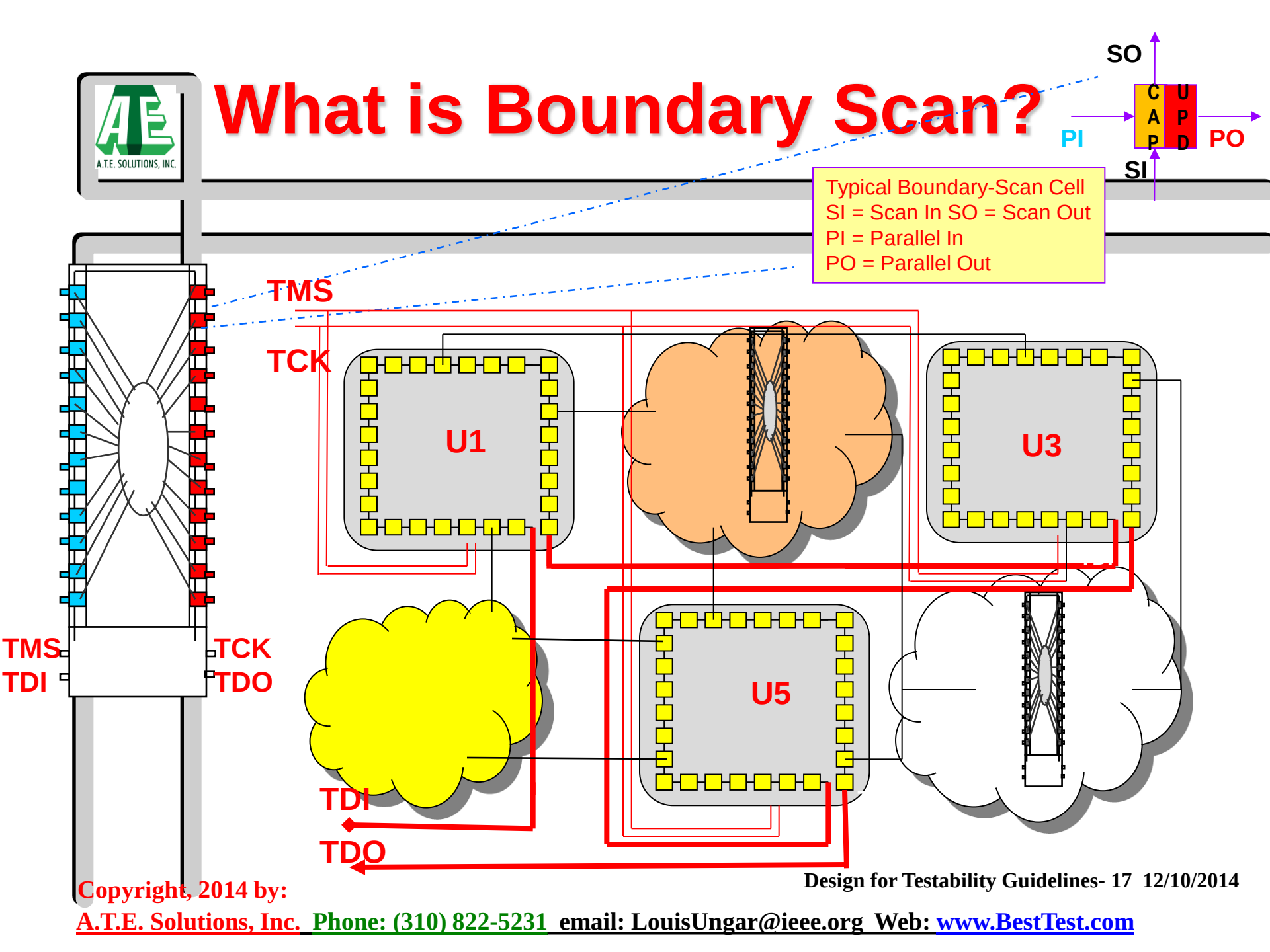
What is Boundary Scan?



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CONSTRUCTION OF THE 1149.1 TEST ACCESS PORT (TAP)

TDI
TDO
TCK
TMS
TRST

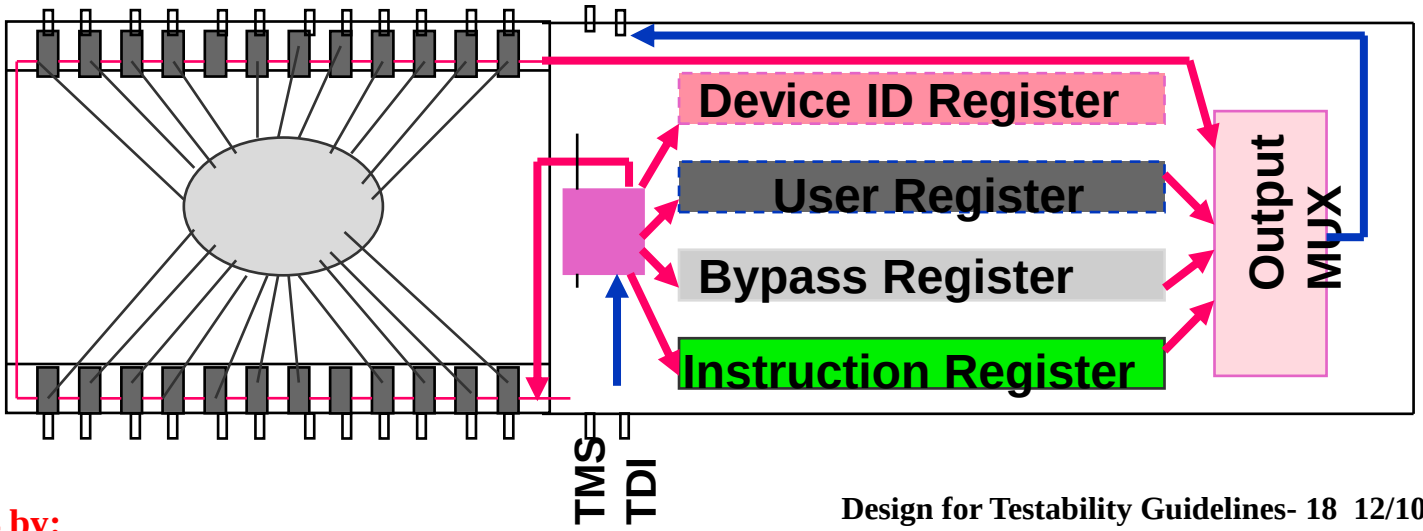
TDI - test data input

TDO - test data output

TCK - test clock

TMS - test mode select

TRST - test reset



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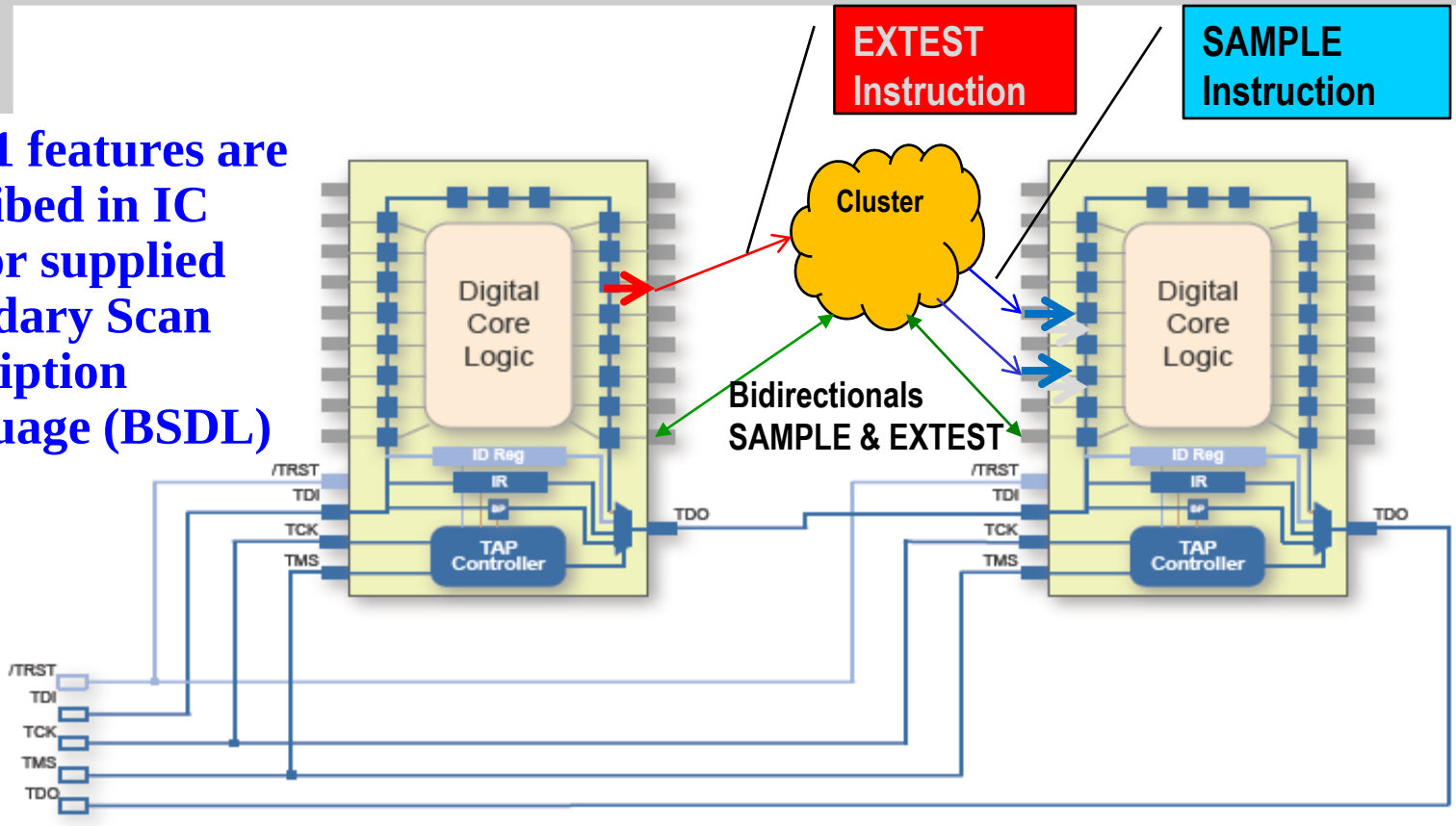
1149.1 Boundary Scan Operation

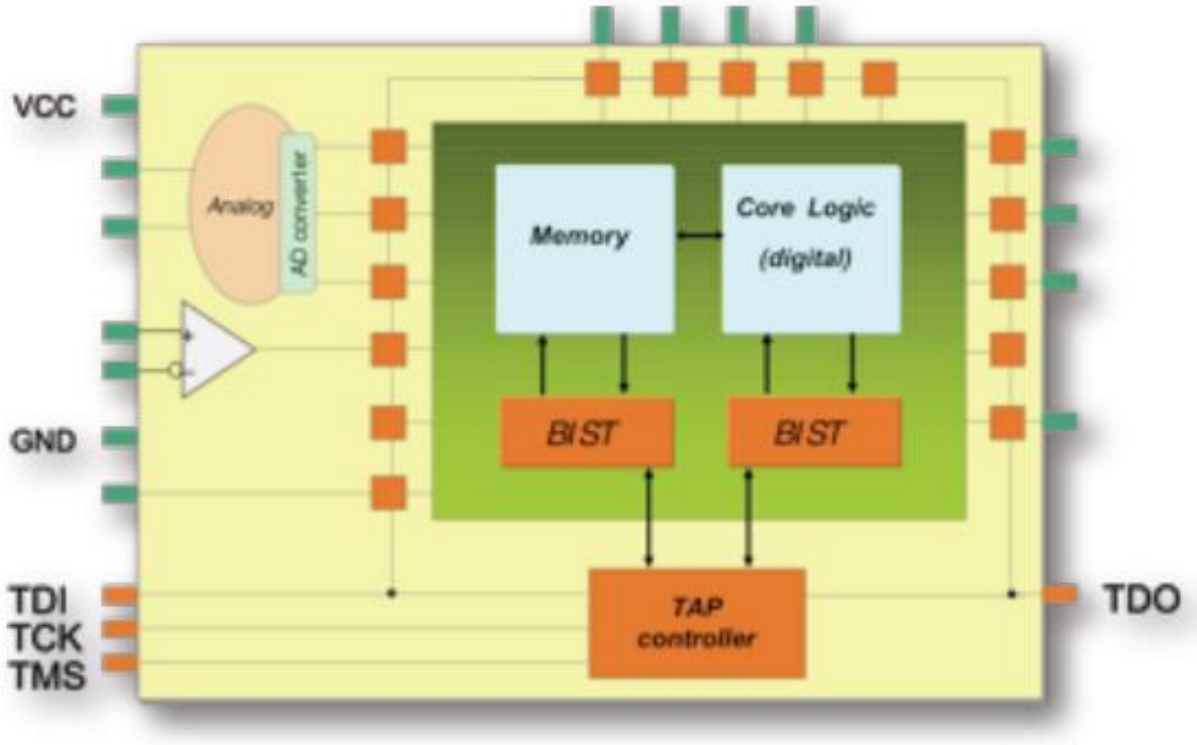
Modified from Goepel JTAG/ Boundary Scan Tutorial

- 1149.1 features are described in IC vendor supplied Boundary Scan Description Language (BSDL)

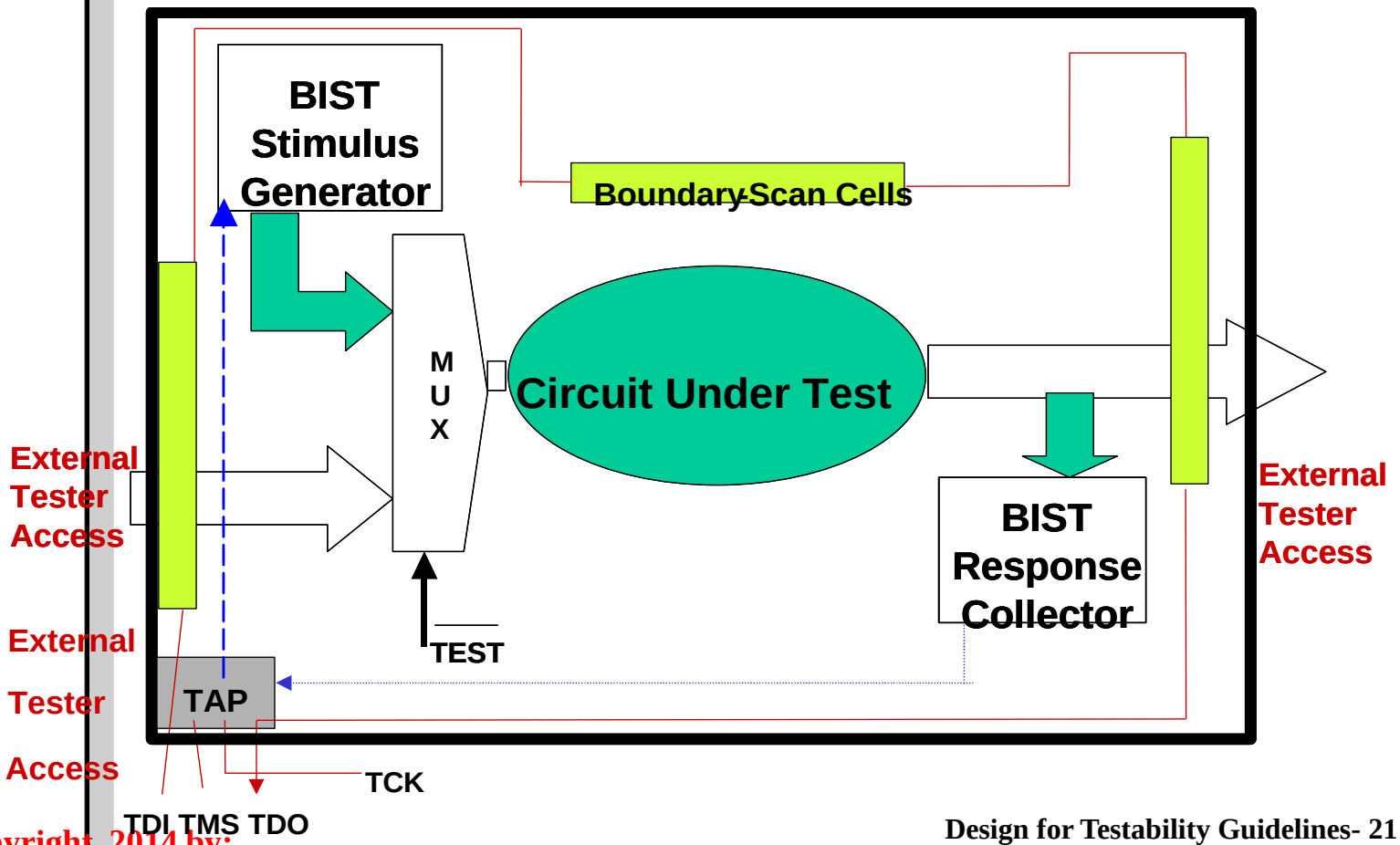


IC Level BIST Controlled by Boundary Scan

Source: Goepel JTAG/ Boundary Scan Tutorial



Board Level BIST with Boundary Scan



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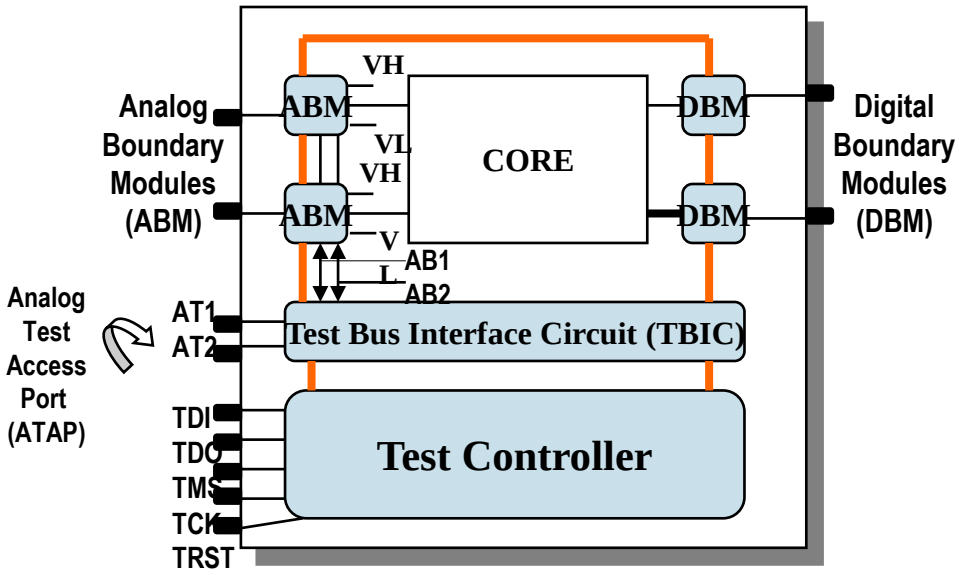
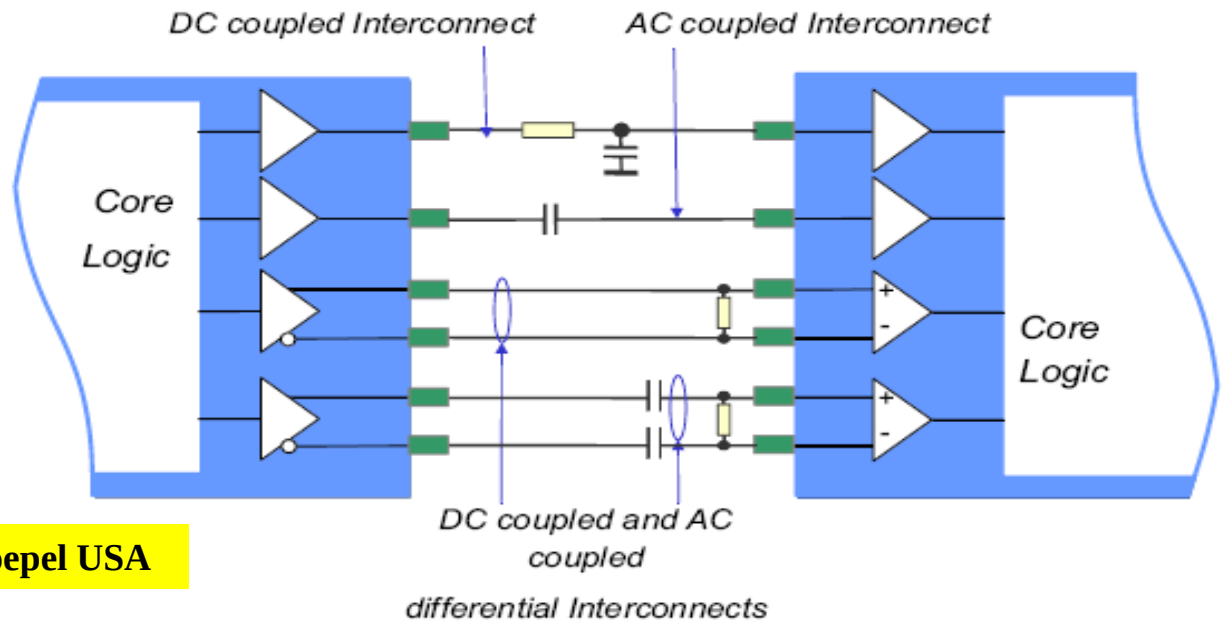
IEEE 1149.4 - Mixed Signal Boundary Scan

- Approved as a full standard in 2001.
- Maintains the 1149.1 protocols, only adds analog capability.
- Still not in use…



IEEE-1149.6 Boundary-Scan Testing of Advanced Digital Networks



Source: Heiko Ehrenberg Goepel USA

Shown above are just a few sample coupling schemes
Coupling capacities could also be implemented inside the IC

- **Approved in 2003, it extends interconnect test to AC-coupled networks by providing**
  - » **Differential interconnections**
  - » **AC coupled networks**
- **Defines hardware structure and two new instructions**
  - » **The EXTEST_PULSE**
  - » **The EXTEST_TRAIN**
- **Well supported and widely used**

IEEE-1149.7 Reduced-pin and Enhanced-functionality Test Access Port and Boundary Scan Architecture

- **Benefits:**
  - Reducing the number of pins
    - » Only 2 pins needed for the TAP instead of 4 (or 5)
  - Improved support for devices with multiple cores
  - Increased debug performance
- **Major Features (besides lower pin count)**
  - Advanced power management features
  - Star topology
  - Chip level bypass and Individual device addressing

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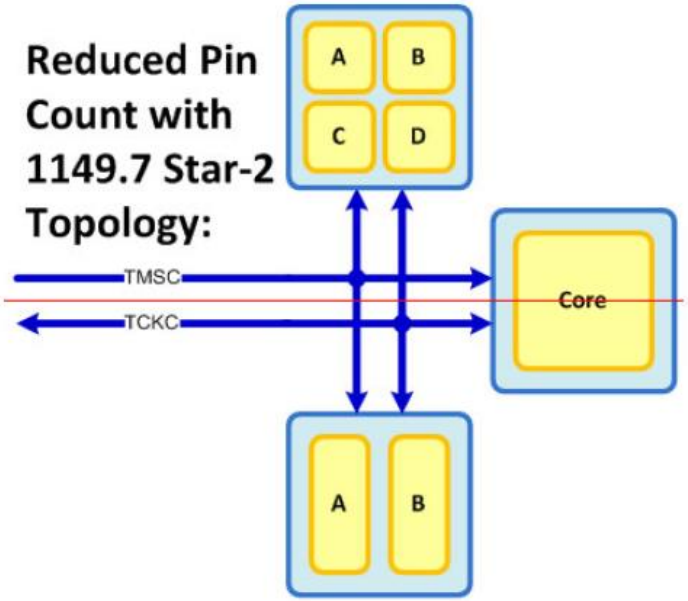
1149.7 Star Topology and Chip-Level Bypass

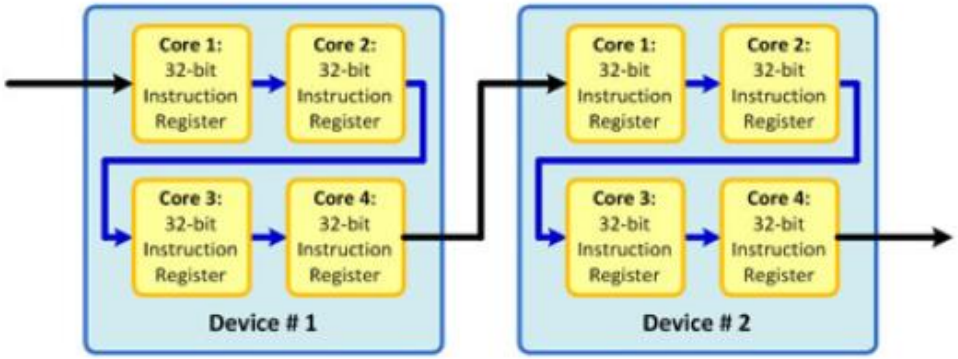
Source: Corelis

Star Topology

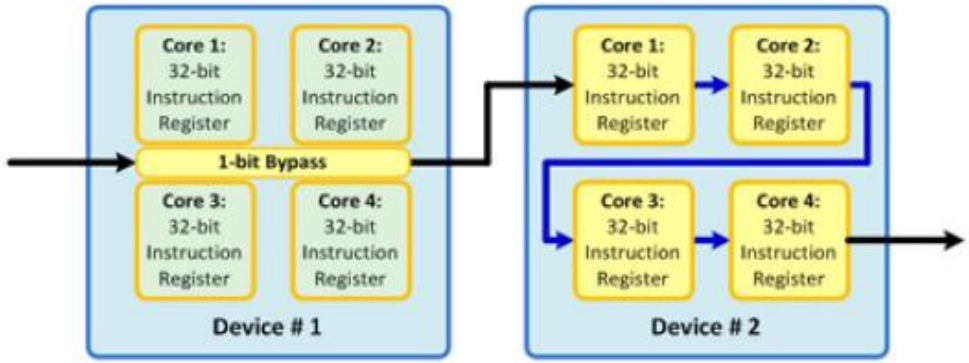
Reduced Pin Count with 1149.7 Star-2 Topology:



Scan Chain Without Chip Level Bypass:



Equivalent Scan Chain With IEEE 1149.7 Chip Level Bypass:

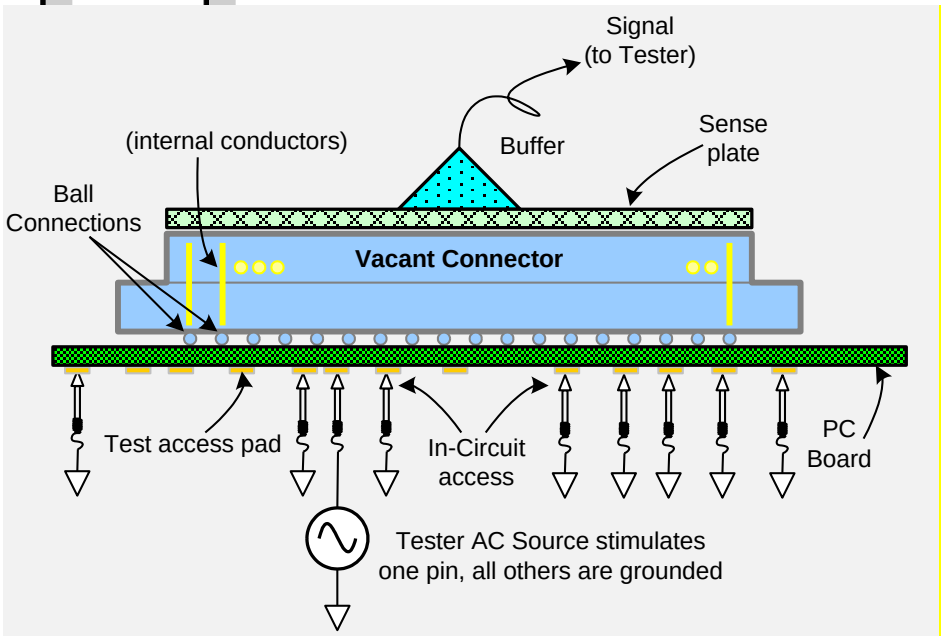


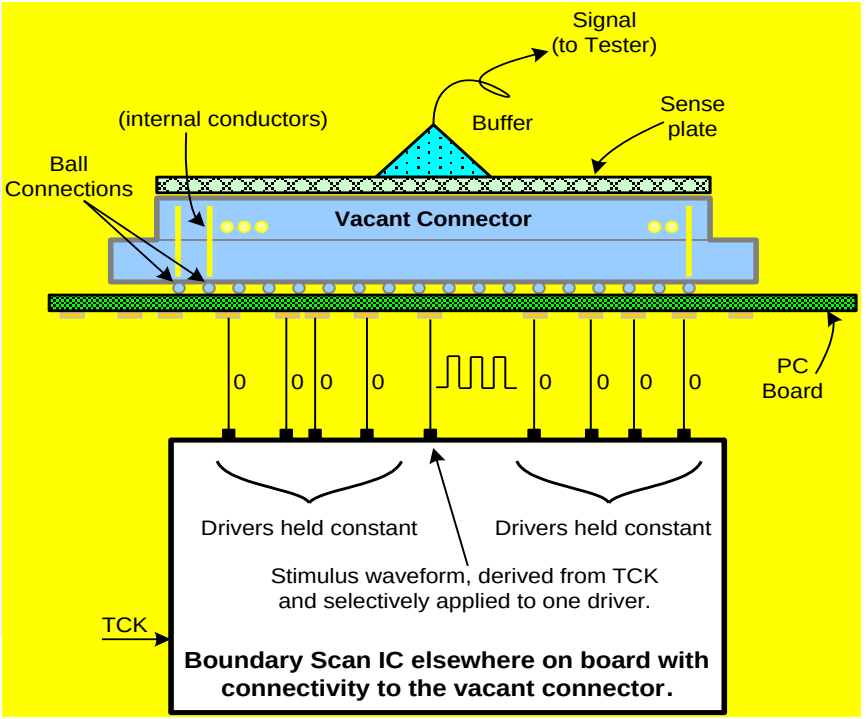
IEEE-1149.8.1 Boundary Scan Based Stimuli of Interconnections to Passive and/or Active Components

Source: SMTA/TMAG Testability Guidelines TP101E, 2014

- **Traditional Vectorless Test (Capacitive Opens Testing)**
- **Using IEEE 1149.8.1 Boundary Scan Stimuli**

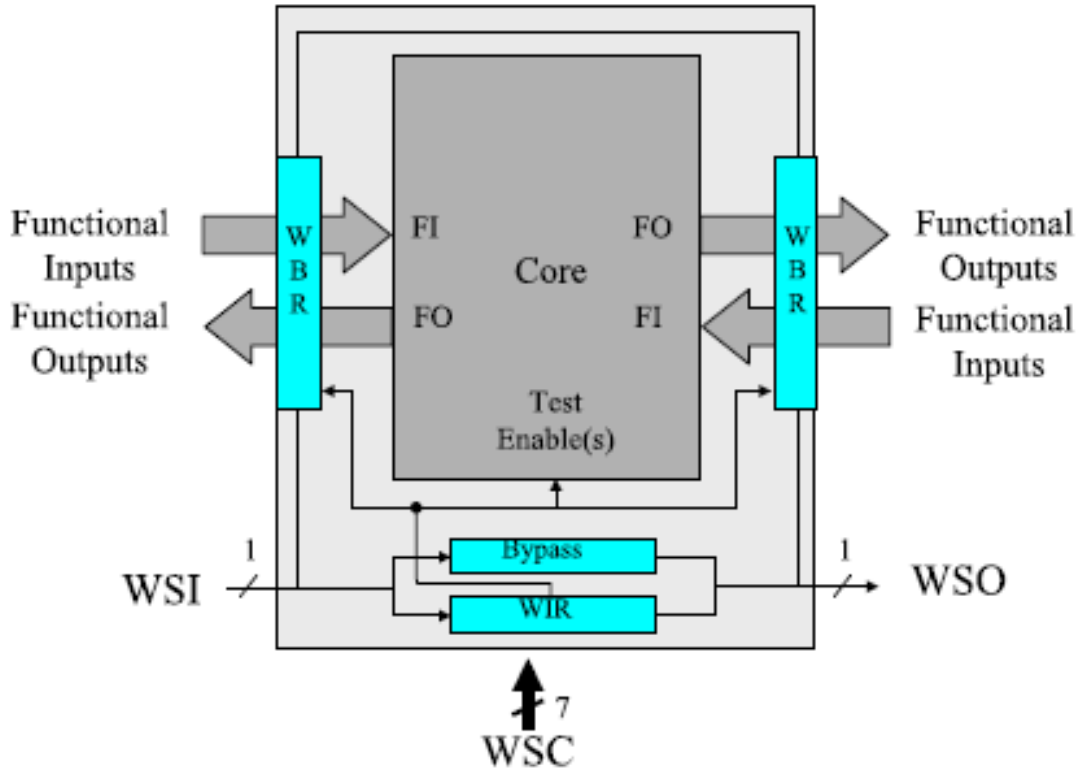
Standard released in 2012





IEEE-1500 Boundary Scan for System on Chip (SoC)

DaSilva, Zorian, Whetsel , Arabi, Kapur, Overview of the IEEE P1500 Standard , ITC 2003



Approved in 2005, the IEEE-1500 hardware architecture comprises

- **Instruction Register**
- **Wrapper Instruction Register and two data registers**
- **Wrapper Bypass Register (WBY)**
- **Wrapper Boundary Register (WBR).**
  - » **The use of Core Data Registers (CDRs) is also anticipated by the standard.**

IEEE-1500 Instructions

DaSilva, Zorian, Whetsel , Arabi, Kapur, Overview of the IEEE P1500 Standard , ITC 2003

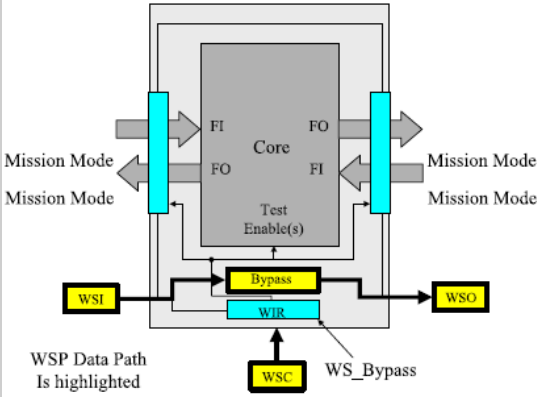


Figure 7: Wrapper configuration during the WS_Bypass instruction

■ **BYPASS**

■ **EXTEST**

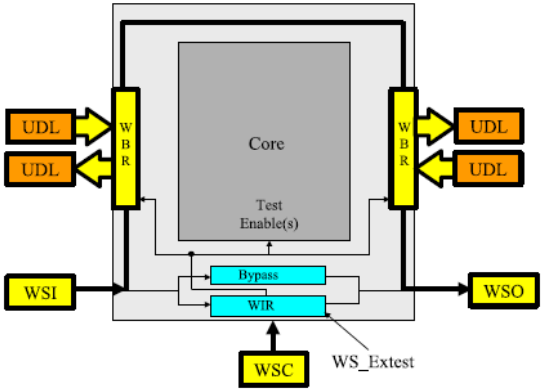


Figure 9: Wrapper configuration during the WS_Extest instruction

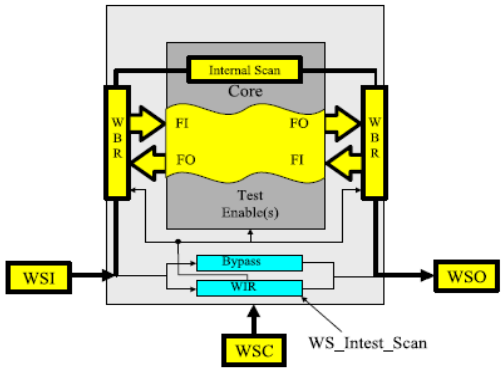


Figure 8: Wrapper configuration during the WS_Intest_Scan instruction

■ **INTEST**

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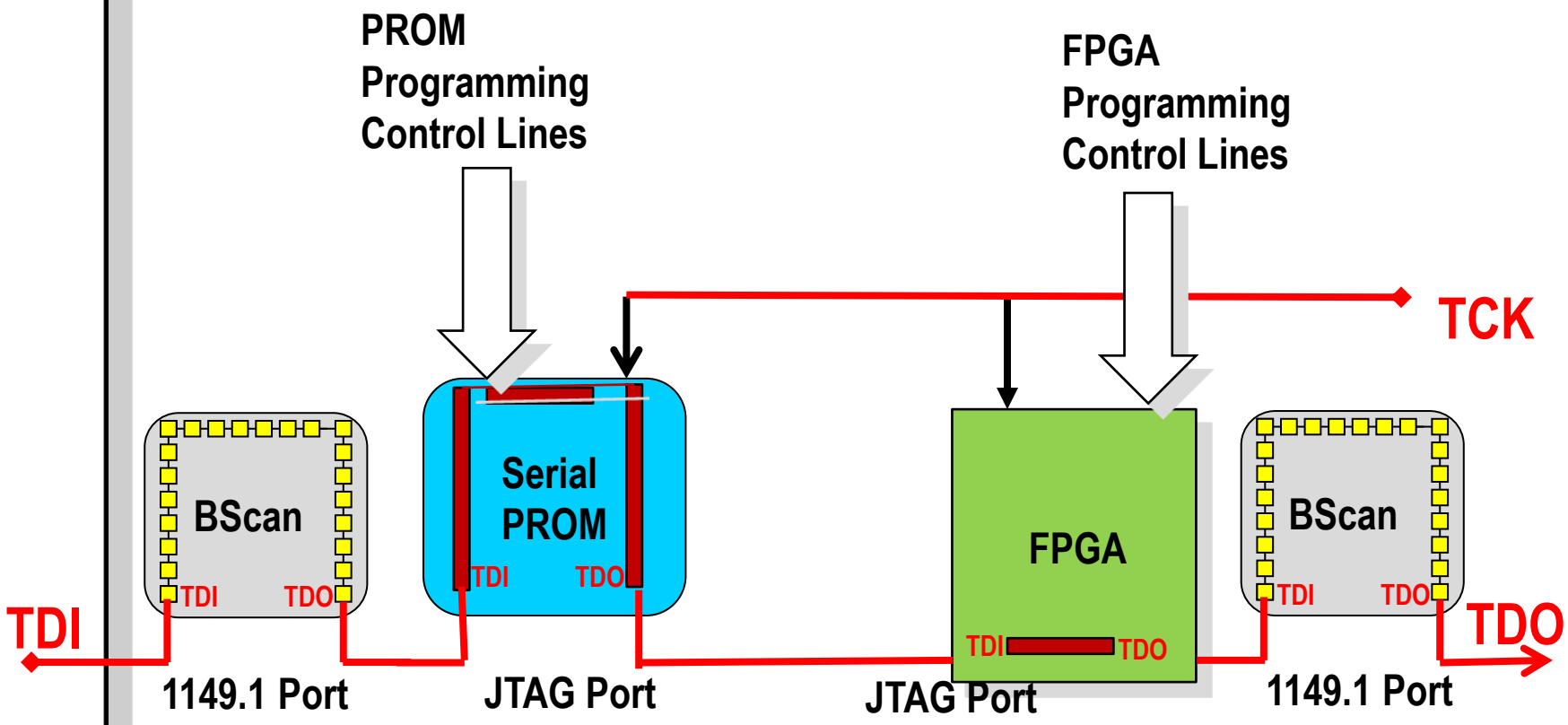
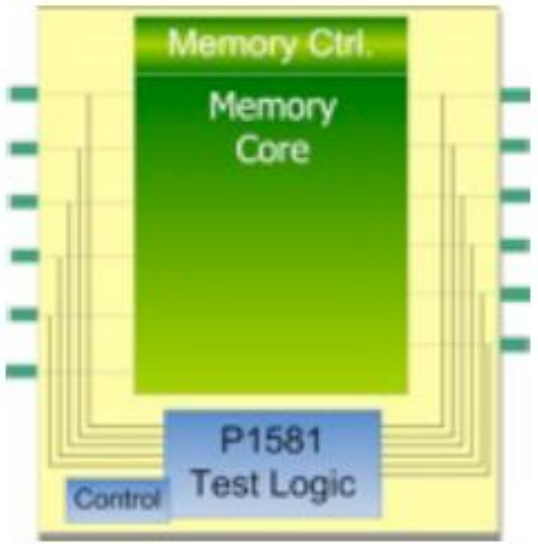
IEEE 1532-2002
In-System Configuration of Programmable Devices Standard



IEEE-1581 Static Component Interconnect Test Protocol and Architecture

- Approved in March 2011 it provides a means for a standard test methodology for memory interconnect testing.
- Describes test circuitry to be implemented in a memory device that bypasses the memory block itself and instead provides a logic connection between input and output pins (using simple logic gates).
- By stimulating the memory input pins and observing its output pins via boundary scan devices connected to the memory, board level connectivity can be verified.



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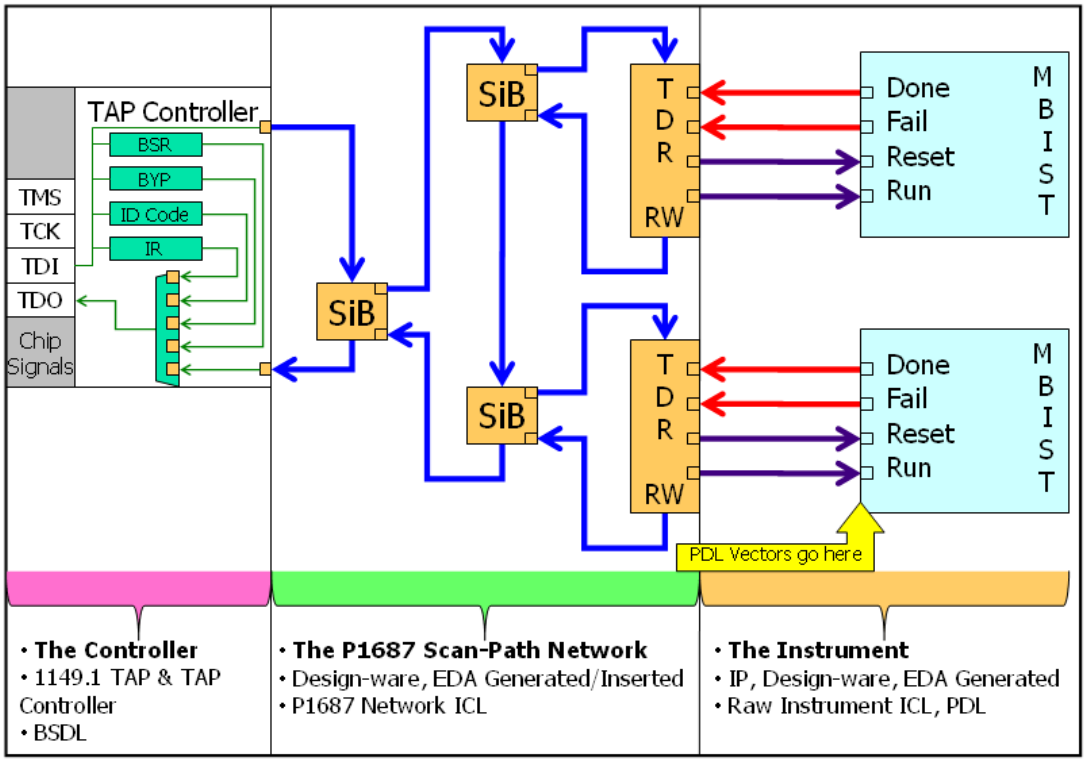
IEEE-1687 Architecture

From: Asset Intertech White Paper, 2013



- **Internal JTAG (IJTAG) Standard for Embedded Instruments became a standard in 2014. Includes**
  - A chip's boundary-scan TAP controller,
  - The device's internal IJTAG scan path network
  - Portable interface for the embedded instrument.
  - Segment Insertion Bit (SIB)
    - » Acts as a gate
    - » Allows on-demand access to instrument interface registers

Benefits from IEEE-1687

- **Allow test reuse**
  - IC level test run at board and system levels
  - Reduce test development costs to a single source
- **Improve diagnostics**
  - Reduce cost of diagnosis
  - Improve fault localization
- **Improve repair management**
  - Deep diagnoses available in the field, but repair is done in the factory

Design for Testability Guidelines and Standards

- Military Standards, Guidelines and Handbook
- IEEE Standards with Boundary Scan
- **SMTA/TMAG Testability Guidelines**
  - » Probing and Fixturing
  - » Flying Probe
  - » Vectorless Test and IEEE-1149.8.1
  - » Automatic Optical Inspection (AOI) and X-ray (AXI)
  - » Electrical (Ad hoc DFT rules)
  - » Analog, Boundary Scan, BIST and System Level Diagnoses
- IPC Design for Excellence (DFX) Guidelines
- Commercial Guidelines
- Emerging and Future Efforts

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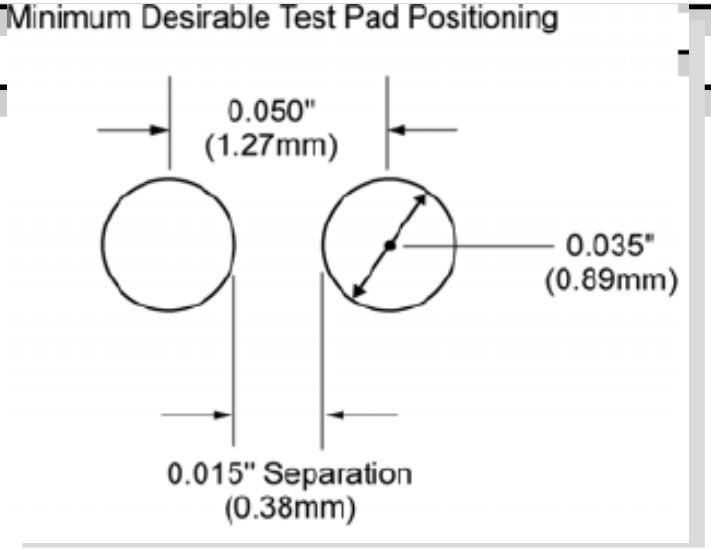
Source: SMTA/TMAG Testability Guidelines TP-101E

Test Pad Positioning



Priority	Target Size	Comments
1	0.035”	Provides most ideal target size.
2	0.035” top 0.030 bottom	Provides an acceptable target size when proper tooling holes are available.
3	Less than 0.030”	Can be used but contact repeatability will be sacrificed. Test fixture will require probe guide increasing cost.

Flying Probe Testers

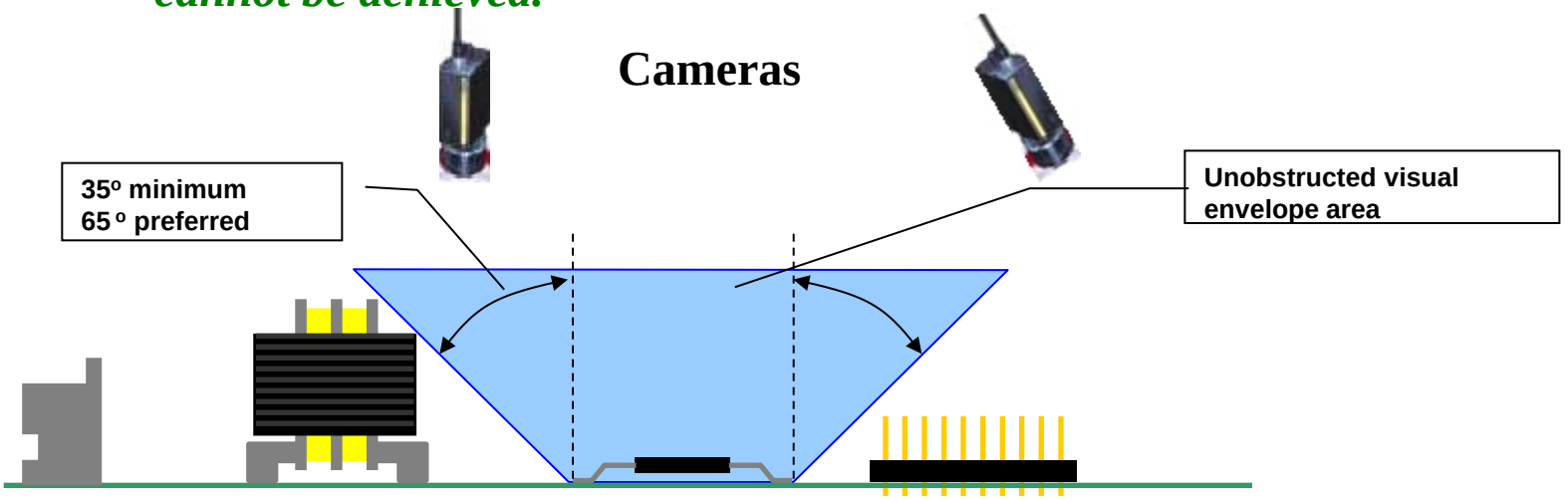
Source: SMTA/TMAG Testability Guidelines TP-101E

- Flying probe testers can reliably hit test points with 0.025 in (0.64mm) diameters with 0.025 in. spacing.
  - » Test vias and pads should be at least 0.014 in and have a 0.014 in free area, and should be accessible from one side of the board.
- Avoid probing large via holes
- Select the appropriate probe tip style
- Use board support to prevent flexing
- Optimize flying probe test times
  - » e.g. Provide fixed access to large pin count nodes, such as ground and power nodes, on the PC board.

Automated Optical Inspection (AOI) Guidelines

Source: SMTA/TMAG Testability Guidelines TP-101E

- *Provides 18 "Design for Inspectability" Guidelines*
- *The combination of lighting and camera access requirements suggest an ideal 65-degree angle from vertical of unobstructed space.*
- *A minimum of 35 degrees is recommended when the full 65 degrees cannot be achieved.*



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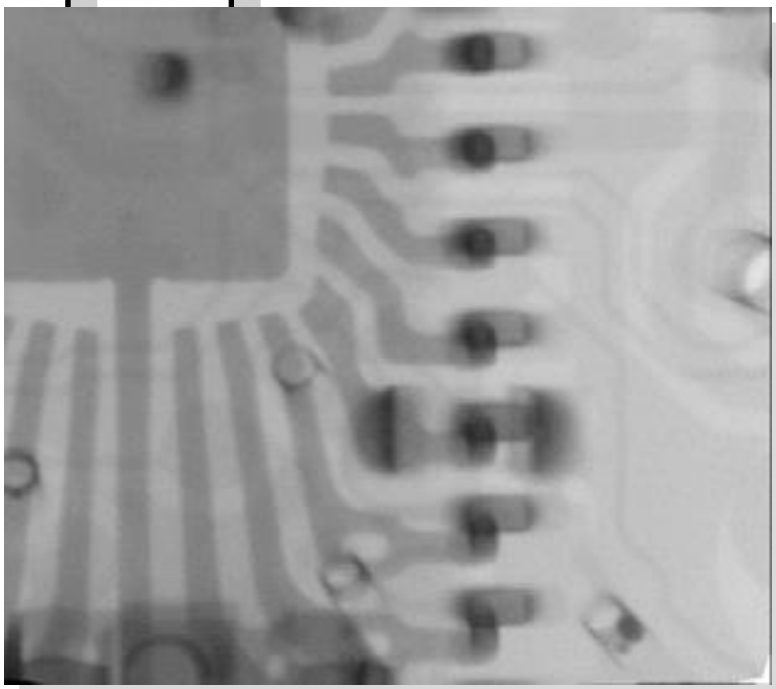
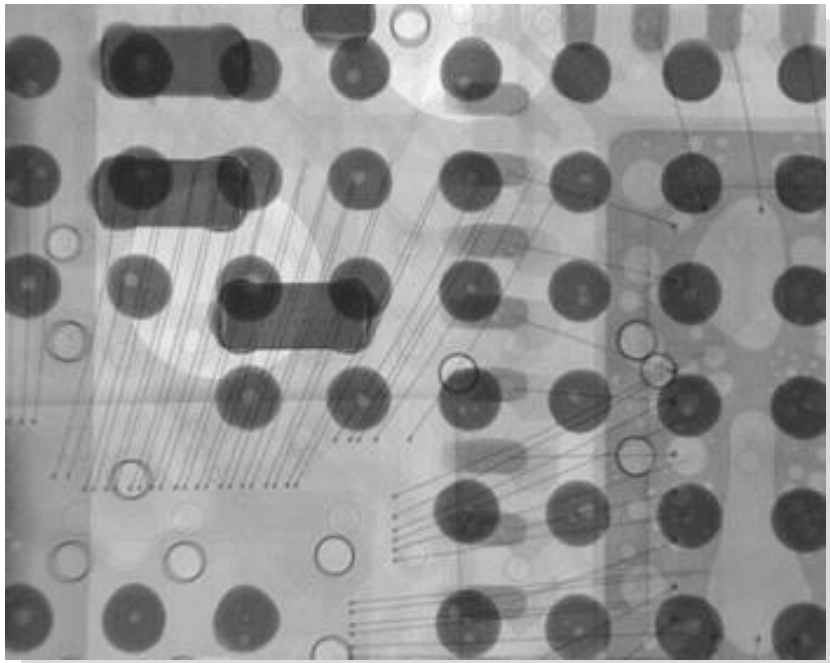
Minimize overlapping solder joints on double sided boards

Source: SMTA/TMAG Testability Guidelines TP-101E

Cross-Section
Automatic X-ray Inspection (AXI)



Manual X-ray (MXI)
Uses Transmission X-ray



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Design for Testability Guidelines and Standards

- Military Standards, Guidelines and Handbook
- IEEE Standards with Boundary Scan
- SMTA/TMAG Testability Guidelines
- **Commercial Guidelines - (Several at IC level)**
  - **IC Level - About a half dozen scan, DFT and ATPG vendors**
  - **Boundary Scan – About a dozen Boundary Scan tool makers**
  - **General Board Level - ASTER's TestWay, others?**
  - **System Level - DSI's eXpress, QSI's TEAMS, others?**

A.T.E. Solutions' The Testability Director ™ includes hundreds of guidelines for ICs, Boards, Boundary Scan, System, Analog, BIST, etc.

- IPC Design for Excellence (DFX) Guidelines
- Emerging and Future Efforts

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Overall Worksheet

- Title Sheet
- User's Guide
- Section Titles
- Section Weight Assignment
- Overall Testability Score

The Testability Director (TM)

Version 3.3

Company:

Product :

Analyst:

Date:

Stored as: Revision:

USERS' Guide:

1. Assign values of 0-10 to the "Assigned Section Weight" column for each category early in the design. (Management task) (Assign a 0 weight to those which you wish to ignore and 10 to those which are mandatory.)
2. Assign values of 0-10 to individual criteria in each category. (Testability Engineering task).
3. When multiple people are assigning weights and scoring, use different colors for each so you can trace contributors.
4. Place values into the "Total Number" column of each criteria. Hyperlink to the Guidance worksheet or see Users' Manual
5. Place preliminary values into the "Meeting Criteria" column for each criteria. Values should reflect existing conditions.
6. A "N/A" result in any calculation indicates an error. Ensure that the weight is 0 when Total Number cell contains a 0.
7. See overall results on this page. An Overall Testability Score above 80% is very good. Decide on your goal for this value.
8. If results indicate poor testability, revisit criteria with low "Score in Percent."
9. Reevaluate based on improving design attributes of those criteria with low scores. Perform trade-off for best results.
10. As a general rule, consider redesigning rather than changing criterion or section weights.

Start using The Testability Director early in the design and revisit at each design review and design change!

		Assigned Section Weight	Section Score in Percent	Section Weight	Section Weighted Score
G0[illegible]	General Guidelines	10	34%	1050.0	359.2
I00[illegible]	IC and ASIC Level Testability Guidelines				
I10000	VLSI, ASIC and Microprocessor Circuit Gu[illegible]elines	8	80%	1368.0	1098.1
I30000	Memory and Programmable Circuit Guideli[illegible]s	6	85%	450.0	383.5
I50000	Structured Design for Testability Guideline[illegible]	9	62%	432.0	266.2
B00000	Board Level Testability Guidelines				
B10000	Inspection				
B11000	Automatic Optical Inspection Guidelines	6	78%	480.0	373.7
B13000	Automated X-Ray Guidelines	8	84%	424.0	313.3
B30000	Connectivity Guidelines				
B31000	Flying Probe Connectivity Guidelines	6	92%	462.0	425.3
B33000	Vectorless Test Guidelines	7	81%	259.0	208.6
B35000	Boundary-Scan Connectivity Guidelines	9	82%	261.0	213.8
B50000	In-Circuit Board Testability Guidelines				
B51000	In-Circuit Test and Testability Guidelines	8	88%	1760.0	1554.9
B53000	Boundary-Scan In-Circuit Testability Guidelines	8	82%	536.0	437.4
B70000	Functional Board Test and Testability Guidelines				
B71000	Digital Circuit Guidelines	7	93%	1575.0	1460.7
B73000	Analog Circuit Guidelines	5	87%	410.0	355.3
B75000	Board Level Boundary-Scan and BIT Guidelines	7	80%	1099.0	875.2
S00000	System Level Testability Guidelines				
S01000	General System Level Guidelines	8	83%	736.0	611.7
S03000	System Level BIT Guidelines	8	[illegible]	1192.0	1051.0
	Totals			[illegible]2494.0	9987.7
Overall Testability Score			80%		

Where to Improve Testability

http://www.besttest.com/OurProducts/TestabilityDirector/

Needs to Improve!

The Testability Director

		Assigned Section Weight	Section Score in Percent	Section Weight	Section Weighted Score
G00000	General Guidelines	10	34%	720.0	86.4
B10000	Board Level Inspection Guidelines				
B11000	Automatic Optical Inspection Guidelines	6	78%	480.0	373.7
B13000	Automated X-Ray Guidelines	8	86%	320.0	240.5
B50000	In-Circuit Board Testability Guidelines				
B51000	In-Circuit Test and Testability Guidelines	8	89%	1712.0	1522.9
B53000	Boundary-Scan In-Circuit Testability Guidelines	8	77%	352.0	271.3
B70000	Functional Board Test and Testability Guidelines				
B71000	Digital Circuit Guidelines	7	93%	1575.0	1460.7
B73000	Analog Circuit Guidelines	5	88%	325.0	285.8
B75000	Board Level Boundary-Scan and BIT Guidelines	7	88%	630.0	552.4
S00000	System Level Testability Guidelines				
S01000	General System Level Guidelines	8	85%	640.0	543.8
S03000	System Level BIT Guidelines	8	89%	952.0	850.3
	Overall Testability Score		80%		

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General and Management Guidelines

Hyperlink criteria to extensive guidelines

Criteria Weight assigned by Test

Criteria scoring determined by designers

Find specific items to improve!

General and Management Guidelines

	Back to Overview and Overall	Criteria Weight	Total Number	Meeting Criteria	Score in Percent	Weighted Score
01000	General Guidelines	10				
01007	Are design requirements and specifications clearly documented prior to the start of any design implementation?	9	10	3	30%	27.0
01008	Are DFT assessments made a part of design reviews at the beginning of conceptual, block diagram, and circuit design stages?	9	15	10	67%	60.0
01010	Is the entire development team aware of testability requirements?	8	5	2	40%	32.0
01015	Is a Failure Mode Effects (Criticality) Analysis being performed for each design milestone?	9	15	10	67%	60.0
01017	Are the test strategy and DFT interactively traded-off during the design process?	6	100	75	75%	45.0
01020	Is the test equipment and tester software to be used selected?	4	5		20%	8.0
G01030	Is testability review a part of the design review?	10	3	2	67%	66.7
G01040	Has a Level of Repair Analysis been accomplished?	7	8	2	25%	17.5
G01050	For each maintenance level, has a decision been made for each item on how built-in test (BIT), automatic test equipment (ATE), and general purpose test equipment will support fault detection and fault isolation?	8	100	10	10%	8.0
01060	Is the planned degree of test automation consistent with the capabilities of the maintenance technician?	9	100	10	10%	9.0
G01070	Have testability objectives been determined?	9	100	10	10%	9.0
G01080	Have restrictions been established in meeting testability objectives?	8	100	10	10%	8.0
G01090	Is a complete design documentation available to test engineers in a timely manner?	9	100	10	10%	9.0
	Section Totals	**105**			**34%**	**359.2**

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IPC-2231 Design for Excellence (DfX) Guidelines

- Work in progress, expected release Feb 2015 at APEX conference
- Encompasses
  - » Design,
  - » Validation,
  - » Manufacturability,
  - » Reliability,
  - » Supportability… and

Design for Testability

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Development Phase	Design Activity	Testability Activity
Conceptual Design	Create product specifications	Create test requirements for each product specification, including fault detection, diagnosis, test times, test costs, etc.
Block Diagram	Define partitions between blocks	Ensure that all partitions are controllable and observable to all inspection and test equipment considered. The mix of inspection and test equipment stages should be determined and test resources identified and procured.
Detailed Circuit Design	Electrical design of printed circuit boards (PCBs), including identification and procurement of parts. Trade-off in components.	Ensure that parts with built-in test, such as boundary scan are given preference. Ensure that controllability and observability within the circuit are maintained. Ensure that "inspectability" for AOI and X-ray is considered. Ensure that bed-of-nails, flying probe or boundary scan access to all signals is available. All test program development can start here.
Circuit Design Verification	Ensure circuit performs functions specified within tolerances and accuracies specified	Create and run design verification tests using discrete instruments or ATE. (Note ATE is not necessary as test should only run once and the design verification test is different manufacturing tests. The former looks for design errors, the latter for defects. In some cases manufacturing tests can also be used for field support tests.) Environmental stress screening (ESS) such as HALT and HASS should be performed here. To enable this, the product must be testable.
Manufacturing	PCB Layout	Circuit board accessibility issues need to be addressed to ensure sufficient access by the inspection and test equipment used in production.
Support	Field support and factory returns	Ensure that tests developed for systems accurately identify failing subsystems or parts that can be replaced quickly and easily by end user. While manufacturing tests can be utilized once the product is returned to the factory, field support tests typically utilize built-in test (BIT or BIST) to repair by replacement. Design for BIT must take place as early as the Block Diagram phase.
Prognosis	Product Health Management	Ensure (during the Detailed Circuit Design phase) that there are sufficient monitoring points and mechanisms to ensure that (life critical) product degradations can be detected and diagnosed.

Design for Testability Guidelines and Standards

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- **Emerging and Future Efforts**
  - **System Level – SJTAG**
  - **DFT in 2020**

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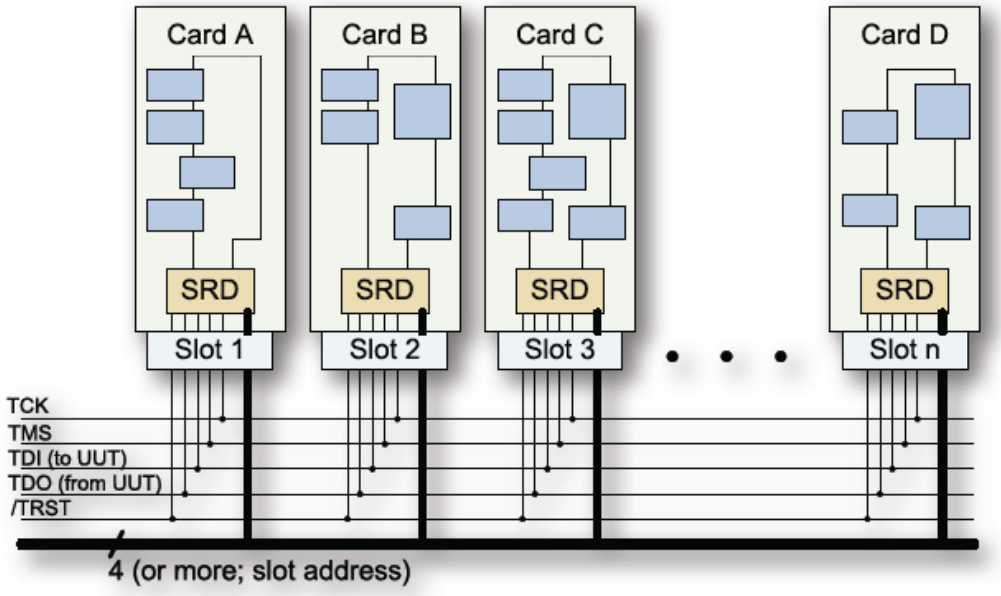
SJTAG and System Level Boundary Scan Chain

Source: Goepel JTAG/ Boundary Scan Tutorial

SRD is Scan Router Device



■ SJTAG

Standardize data contents and formats for communication:

- » between external Test Manager platforms and internal Embedded Test Controllers
  - eXternal Boundary Scan Test (XBST)

and

- » between Embedded Test Controllers and the UUTs they serve
  - Embedded Boundary Scan Test (EBST)

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How will DFT change by 2020?

- **Topics that will likely impact the future**
  - IDDQ Testing of CMOS (boards and systems)
  - SJ BIST from Ridgetop Group - Andrew Levy will cover this next
  - Thermal Imaging for Diagnoses
  - Prognostic Health Management for all electronics
  - No Fault Found (NFF) and False Alarms > 70% of repairs
  - Overcome DFT & BIST security threats
  - Built-In Self Repair and Built-In Self Healing
- **We'll keep you informed through our courses.**

  http://www.besttest.com/Courses/
- **We'll keep The Testability Director updated!**

  http://www.besttest.com/OurProducts/TestabilityDirector/

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THANK YOU

Teşekkürler

Gracias

Merci

Hvala

Obrigado!

Vielen Dank

شكراً

Bedankt

Díky

תודה

Grazie

Ευχαριστώ

ขอบคุณ

Köszönettel

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Existing Test Methods

- Focus on Manufacturing Process
  - Boundary Scan (JTAG / IEEE 1149.1)
  - Optical / X-Ray Inspection
- Focus on Static Measurements
- Reliability Measurements Are Lacking
  - Reliability = Performance over Time
  - Implies field measurement & monitoring
  - Intermittencies develop after deployment

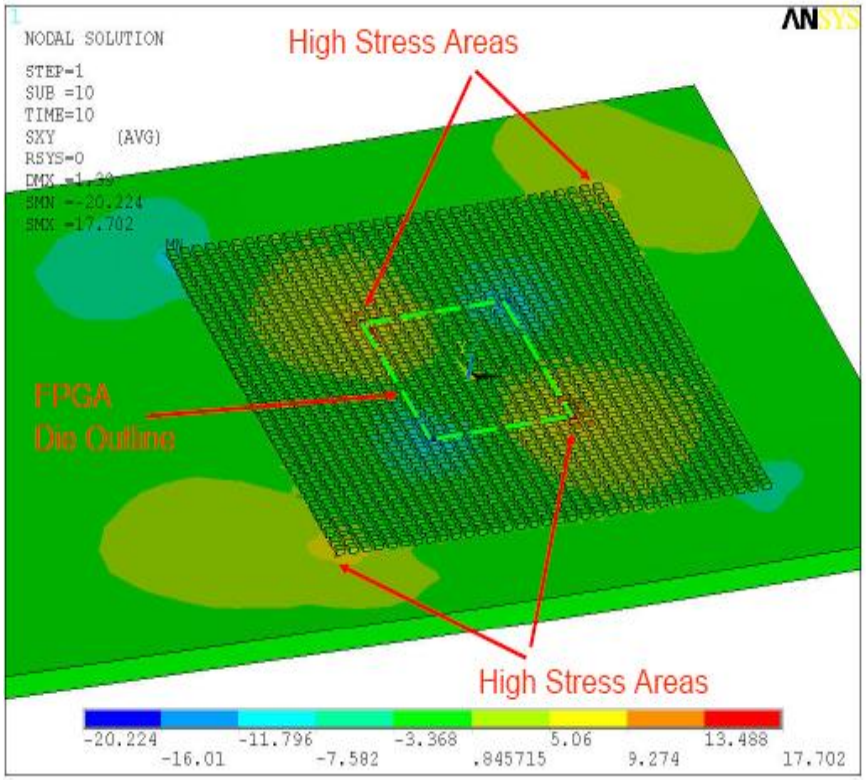
Intermittencies

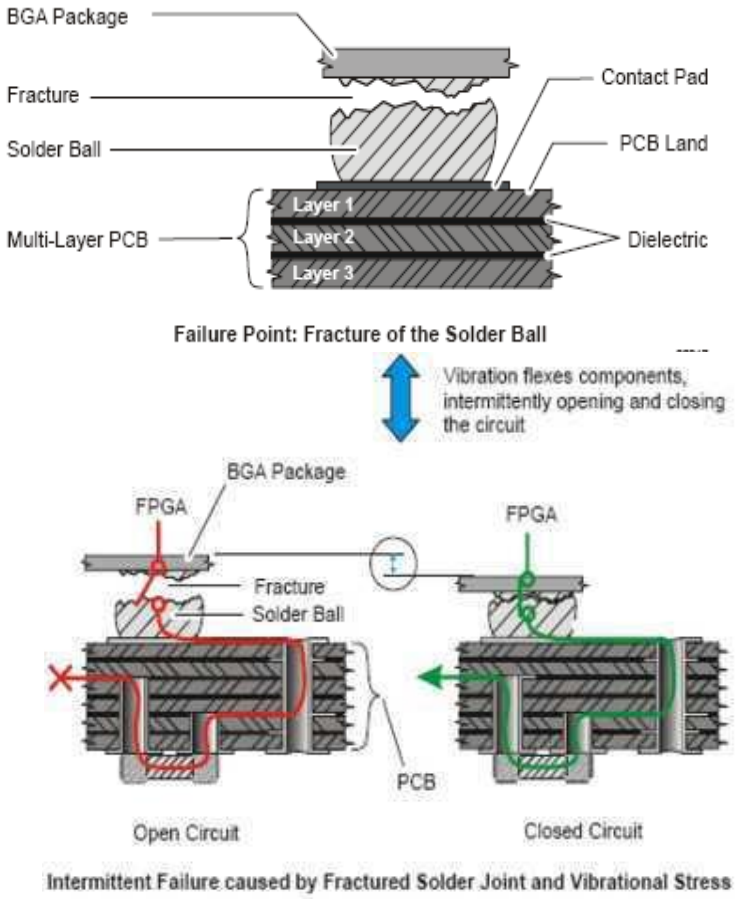
- An interconnect intermittent fault is an event that causes the interconnect resistance to increase for a predefined amount and last for a minimum time.
- Fault detection is linked to # of occurences
- Definition evolved:
  - From: R increase of 1KΩ lasting at least 1µs
    → JEDEC 22-B111
  - To: R increase of 200Ω lasting at least 200ns
- Interconnect is classified as failing if subsequent to the occurence of the first event, nine more events are detected that occur within a period of time T2 that is less than or equal to 10% of the time to the occurrence of the first event T1. (T2 <= 0.1*T1)

Intermittencies

- With present technology, reported electronic system problems in the field cannot be duplicated at the service point or in the lab
- "Three/Four-letter" words (CND, NTF, RTOK)
  - Could Not Duplicate (CND)
  - No Trouble Found (NTF)
  - Retest OK (RTOK)
- 50 to 80% of these CND/NTF/RTOK problem categories are reported by service personnel.
- Major culprits – Solder joint intermittencies and NBTI effects in deep submicron ICs

Defects: Fractures & Intermittency



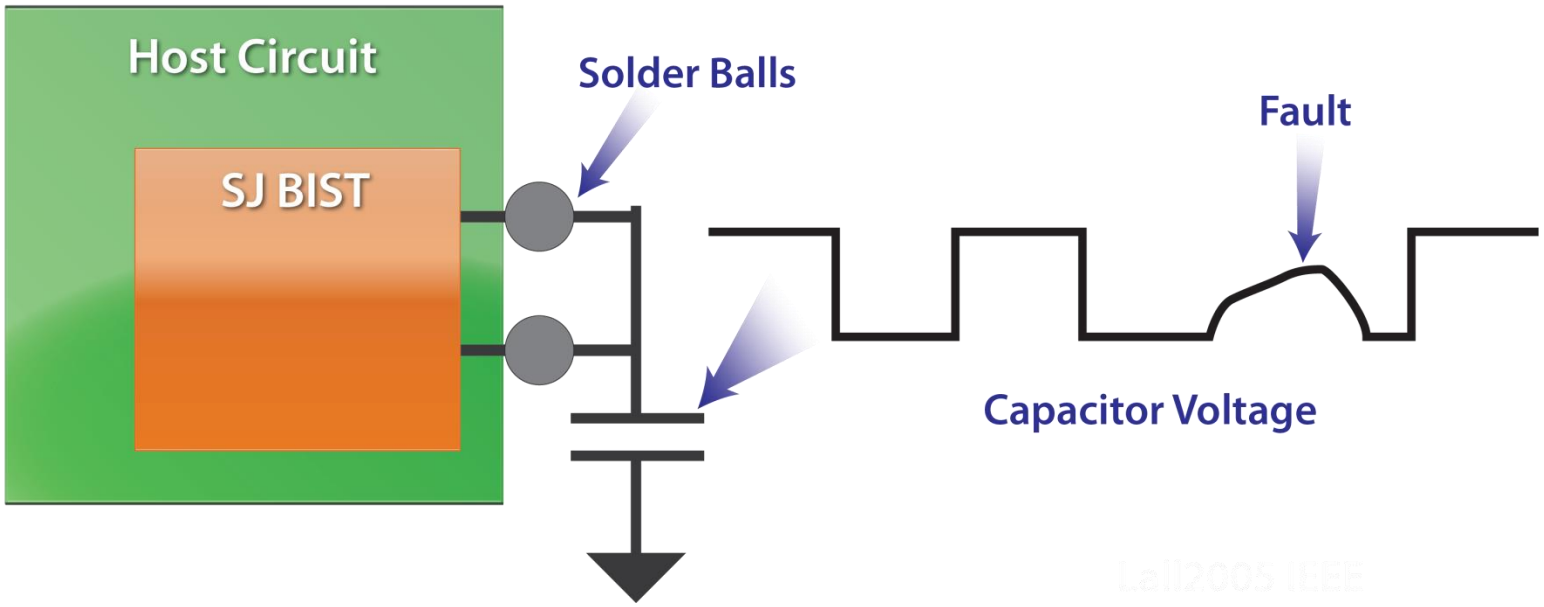


SJ BIST™

- SJ BIST = Solder Joint Built-in Self-Test
  - Verification & validation of solder joint interconnect reliability
    (Methodology applies any type of interconnection)
- Objectives
  - Detection of impending interconnect failures
  - Unique in-situ testing in operating circuits
  - Technology-independent
- Features and Benefits
  - Detects ball fractures prior to catastrophic failure of circuit
  - Provides actionable maintenance data
  - Independently tested and verified
  - Endorsed by leading automotive and aerospace customers
  - Also used for Highly Accelerated Life Test (HALT)
  - Complements standard manufacturing test methods

SJ BIST Operation

- Similar to a simple memory test: W0 – R0; W1 – R1
- Runs concurrently with host circuit
- Verilog/VHDL core (patent pending)
  - Each core tests two I/O pins
  - Pins are externally wired together
  - Optionally small capacitor connected to the two pins



About Ridgetop Group, Inc.

- Incorporated in 2000, and headquartered in Tucson, AZ. Ridgetop Europe established in 2010 in Belgium.
- Microelectronic Design and Test Solutions:
  - SJ BIST™ Based Test Solutions
  - ProChek™ Semiconductor Characterization System
  - Q-Star Test™ Precision Current Measurement Instruments
  - PDKChek™ In-Situ Test Structures
  - ISO:9001/AS9100C-compliant Design and Integration Services
- Strong market position with commercial and government customers in USA, Canada, Europe, and Asia

Ridgetop Group Facilities in Tucson, AZ

Ridgetop Europe Facilities in Brugge, Belgium

Questions?

- Slides and recording of the webinar will be available shortly via an e-mail from Ridgetop
- E-mail follow-up questions & comments to
  - Louis Ungar: louisungar@ieee.org
  - Andrew Levy: andrew.levy@ridgetopgroup.com
- Please fill out our brief feedback survey at: https://www.surveymonkey.com/s/RCFP27Y

Thank you!

Ridgetop Group, Inc.

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